CoaXPress Multi-Device Multi-Stream Host IP 1.1.1

Xilinx & Intel FPGA Core IP

EASii IC

CoaXPress Host IP from EASii-IC enables the connection of 1 to 8 CoaXPress devices, each transmitting multiple high-speed video streams of 1 or more cameras over coaxial cables. The CoaXPress standard enables the transmission of video-streams over 40 meters at a maximum transfer rate of 25 Gbps per device or over 200 meters at a maximum transfer rate of 5 Gbps per device. Each coaxial cable provides a high-speed downlink connection video transfer rate from 1.25 Gbps to 6.25 Gbps and a low-speed uplink connection at 20.83 Mbps for communication and control.

ABOUT COAXPRESS

CoaXPress standard defines a cost effective and easy interfacing between video devices and acquisition hardware over RG59 and RG6 coaxial cables. It enables hot-plug of devices and 24V power-over-cable with up to 13 Watts per cable.

A device can support multiple cameras of many video stream formats. Video streams are sent to a host at a selectable high-speed downlink connection rate from 1.25 Gbps to 12.5 Gbps per cable, with up to 8 cables per device to increase the total bandwidth to 100 Gbps.

Device and cameras can be controlled from a host through the uplink connection at 41.66 Mbps. The standard also provides a low latency, accurate trigger interface between device and host.

CoaXPress supports GenICam international standard, providing a generic programming interface for all kinds of cameras regardless of the interface technology.
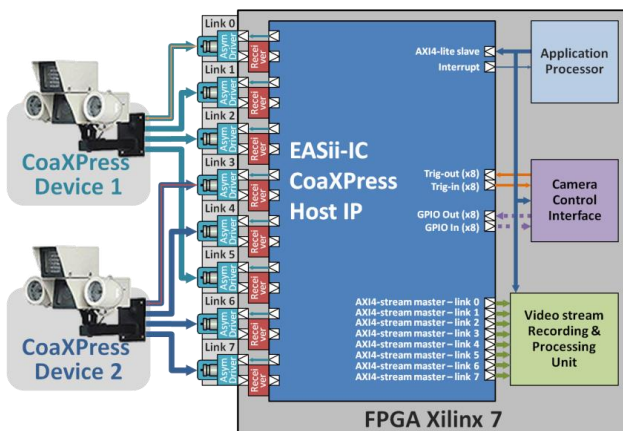
APPLICATIONS AND DOMAINS

Vision systems requiring

- High-resolution and high-speed digital cameras
- Real-time image acquisition
- Pixels on target
- Long distance cables with excellent EMI/EMC performance

Domains

- Machine vision
- Military and aerospace
- Aerial mapping and traffic management
- Security

TYPICAL USE CASE

EASII IC CXP HOST CORE IP FEATURES

- JIAA CXP-001-2013 CoaXPress 1.1 compliant
- Hardware-based Automatic Discovery
- with software interface enabling manual link configuration
- Independent downlink connection rates, from 1.25 Gbps to 6.25 Gbps
- Up to 8 coaxial connections per Host IP, enabling all con-nection topologies, from 1 to 8 devices of 1 to 8 connections each
- Supports multiple video-streams per device, for a total of up to 256 independent stream IDs per Host IP
- Supports all GenICam compliant image formats: rectangu-lar and arbitrary shaped, area and line scan, single and mul-ti tap, multiple regions of interest, all standard pixel for-mats
- Hardware-based video-stream management: automated error detection and recovery at image-level
- AXI4-stream interface per downlink for video streams run-ning at up to 200 MHz
- Trigger in/out interface with uplink latency of 3.4μs
- Optional 8in/8out GPIO interface compliant with JIIA NIF-001-2010 CoaXPress 1.0 standard
- Slave AXI4-lite processor interface for application specific control between host and cameras
- Xilinx7 series and UltraScale compatible, IP-XACT support

PRODUCT DETAILS

- Free connection topology of 1 to 8 devices, of 1 to 8 coaxial cables each for a total of 8 coaxial cables, with independent downlink bit-rate per device
- Dynamic device connection reconfiguration
- Embedded CRC management and error correction
- Video-stream data packet size up to 4096 bytes
- Video-stream interface AXI4-stream master 32-bit
- Embedded video-stream management: image-level error detection and interface for image format monitoring
- Embedded management of triggers and optional GPIOs per device
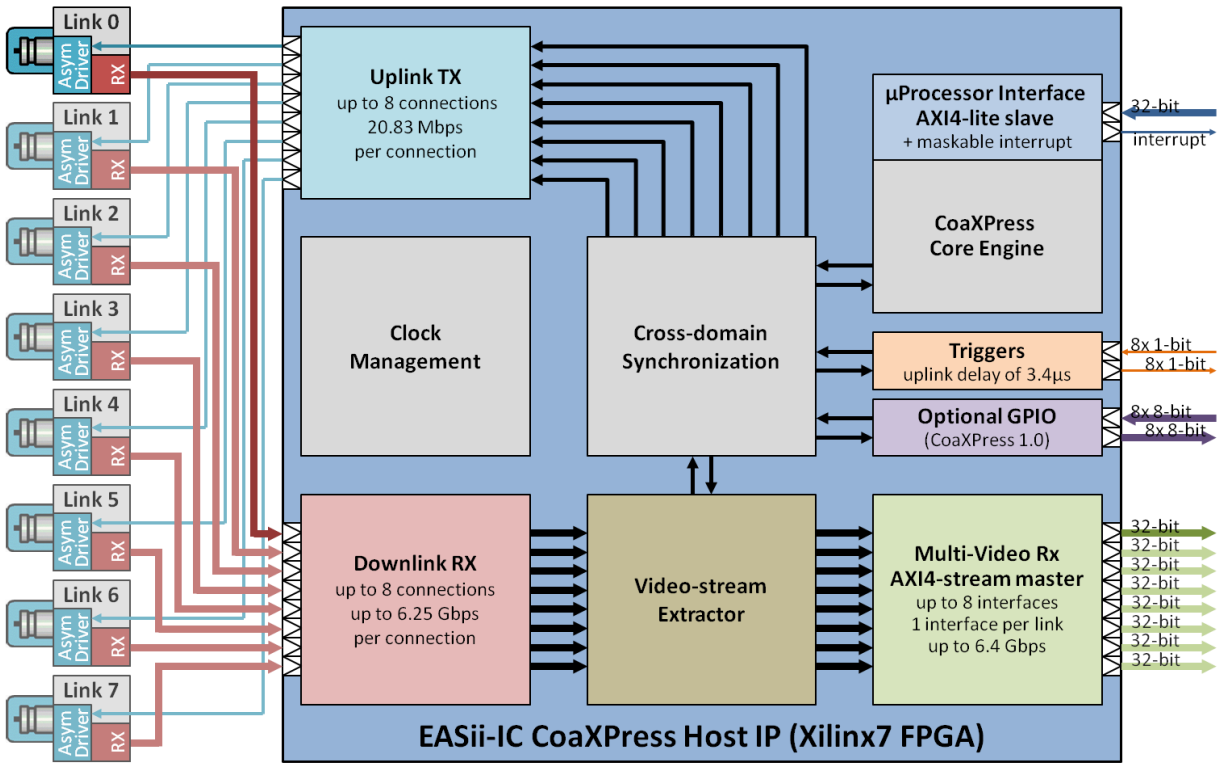- μProcessor interface AXI4-lite slave 32-bit

DELIVERABLES

- Single or multi-use license
- Encrypted source code: VHDL RTL with synthesis scripts for Xilinx Vivado or Intel Quartus
- Comprehensive documentation package: specification, integration, IP-XACT component, etc.
- Integration test-suite

Xilinx & Intel FPGA Core IP

CORE IP ARCHITECTURE

Diagram labels:
- Link 0, Link 1, Link 2, Link 3, Link 4, Link 5, Link 6, Link 7 (Asym Driver / RX)
- **Uplink TX** — up to 8 connections, 20.83 Mbps per connection
- **Clock Management**
- **Cross-domain Synchronization**
- **Downlink RX** — up to 8 connections, up to 6.25 Gbps per connection
- **Video-stream Extractor**
- **µProcessor Interface AXI4-lite slave** + maskable interrupt — 32-bit, interrupt
- **CoaXPress Core Engine**
- **Triggers** — uplink delay of 3.4µs — 8x 1-bit, 8x 1-bit
- **Optional GPIO** (CoaXPress 1.0) — 8x 8-bit, 8x 8-bit
- **Multi-Video Rx AXI4-stream master** — up to 8 interfaces, 1 interface per link, up to 6.4 Gbps — 32-bit (x8)
- **EASii-IC CoaXPress Host IP (Xilinx7 FPGA)**

CORE IP RESSOURCES

Core IP Resources on 7-series	1 link	2 links	4 links	8 links
Number of coaxial links	1 link	2 links	4 links	8 links
Flip-flops	6346	11386	21626	42718
LUT	6105	10714	19688	40122
BRAM36Kb	15.5	25.5	45.5	85.5
Clock trees	3	4	6	10
DSP48	2	3	4	9

CONTACT US

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