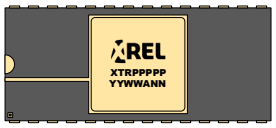
XTR40010

High Temperature Isolated Two-Channel Transceiver

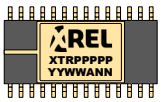
Rev 3 – August 2021 (DS-00400-13)

Data Sheet

PRODUCTION



DIP28
XTR40011



SOIC28
XTR40011

SOIC16
XTR40012

FEATURES

- Supply voltage 3.3V to 5.5V.
- Dual Transmitter/Receiver (TX/RX) channels.
- Operating junction temperature from -60°C to +230°C.
- Data rate up to 4.2 Mbits/second per channel.
- Transient common mode current immunity of 100mA (50kV/µs across 2pF of inter-winding capacitance).
- Hysteresis on digital input for noise immunity.
- Enable control signal on both TX and RX functions.
- OOK (On-Off Keying) modulation.
- 3 bits programmable carrier frequency for EMC compliance.
- Configurable TX and RX modulation polarity.
- Latch-up free.
- Ruggedized SMT packages (CSOIC28).
- Also available as bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- Intelligent Power Modules (IPM).
- Power conversion, power generation and motor drive in aeronautics.
- Isolated gate drive for IGBT, MOSFET, JFET and SiC Transistors
- Isolated sensor interfaces.
- Isolated power inverters.

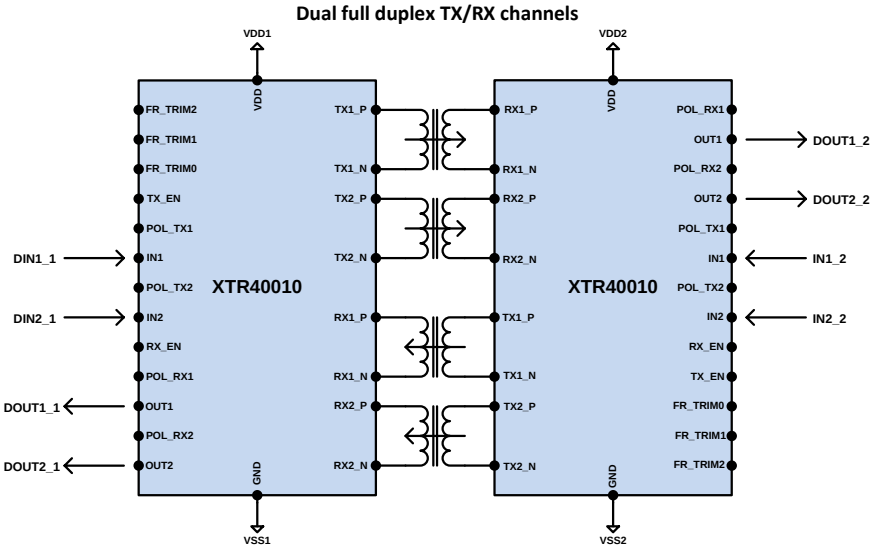
DESCRIPTION

The XTR40010 implements a high-temperature dual-channel (2 TX/RX) isolated data transceiver. It can be used as general-purpose isolated transceiver. It is also well suited for isolated data communication between a microcontroller or a PWM controller, with the intelligent power gate driver XTR26010 or XTR26020. The galvanic isolation is achieved by external high-temperature 1:1 pulse transformers.

The XTR40010 integrates in a single package 2 transceivers (two full duplex channels). The implementation of 2 full duplex TX/RX isolated channels requires 2 XTR40010, one being connected to one side of the transformers and one to the other side. When used with XTR260X0, the XTR40010 allows implementing a 2 full duplex TX/RX channels with only one instance of XTR260X0. Indeed, the XTR260X0 transceiver is fully compatible with the XTR40010. The complete solution is optimized to minimize the size of the transformer, the number of external components, the transmission delay (<120ns) and to maximize the noise margin, even in harsh dV/dt conditions (50kV/µs across 2pF of inter-winding capacitance).

PRODUCT HIGHLIGHT

Dual full duplex TX/RX channels



ORDERING INFORMATION

X	TR	40	010
Source : X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR40010-BD	-60°C to +230°C	Bare Die		
XTR40011-D	-60°C to +230°C	Ceramic side braze DIP	28	XTR40011
XTR40011-S	-60°C to +230°C	Ceramic SOIC	28	XTR40011
XTR40012-S	-60°C to +230°C	Ceramic SOIC	16	XTR40012

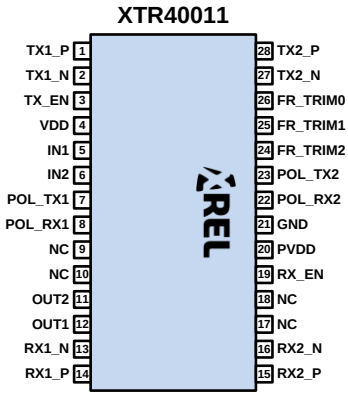
Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

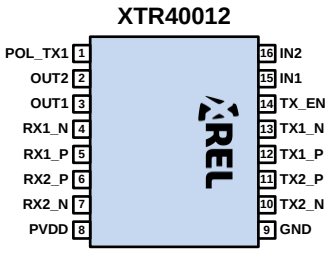
ABSOLUTE MAXIMUM RATINGS

Voltage on any pin, input or output, to GND	-0.5 to 6V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

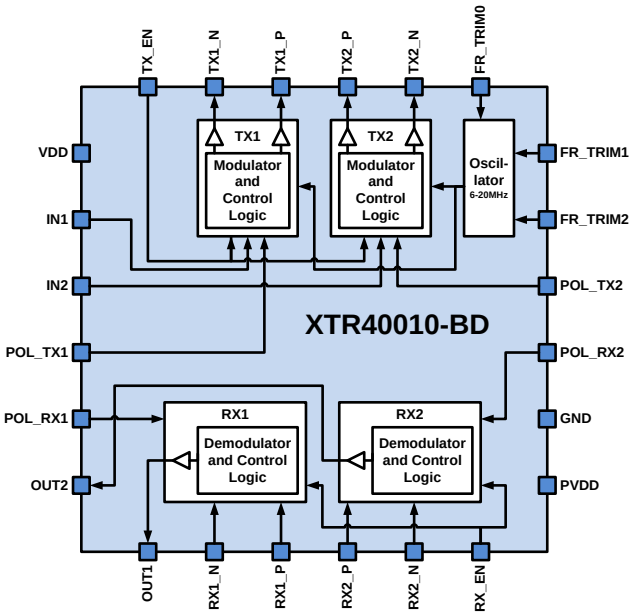
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS





BLOCK DIAGRAM



Die level block diagram showing all available functionalities and bond-pads.

PIN DESCRIPTION (CSOIC28)

Name	Description	Pin number	
		XTR40011	XTR40012
TX1_P	Positive differential output of the transmitter TX1. To be connected to the primary of the pulse transformer.	1	12
TX1_N	Negative differential output of the transmitter TX1. To be connected to the primary of the pulse transformer.	2	13
TX_EN	Digital input transmitter enable pin to be connected to **PVDD** to enable TX1 and TX2.	3	14
VDD	For proper operation this pin must be connected to **PVDD**.	4	8
IN1	Schmitt-triggered digital input of transmitter TX1.	5	15
IN2	Schmitt-triggered digital input of transmitter TX2.	6	16
POL_TX1	Schmitt-triggered digital input that sets the polarity of the transmitter TX1. To be connected to **GND** for non-inverting input or to **PVDD** for inverting input.	7	1
POL_RX1	Schmitt-triggered digital input that sets the polarity of the receiver RX1. To be connected to **GND** for non-inverting output or to **PVDD** for inverting output.	8	↓[1]
NC	Do not connect.	9	-
NC	Do not connect.	10	-
OUT2	Digital output of receiver RX2.	11	2
OUT1	Digital output of receiver RX1	12	3
RX1_N	Negative differential input of receiver RX1. To be connected to the secondary of the pulse transformer.	13	4
RX1_P	Positive differential input of receiver RX1. To be connected to the secondary of the pulse transformer.	14	5
RX2_P	Positive differential output of receiver RX2. To be connected to the secondary of the pulse transformer.	15	6
RX2_N	Negative differential output of receiver RX2. To be connected to the secondary of the pulse transformer.	16	7
NC	Do not connect.	17	-
NC	Do not connect.	18	-
RX_EN	Schmitt-triggered digital input enable pin for the receivers. To be connected to **PVDD** to enable RX1 and RX2.	19	↑
PVDD	Positive power supply	20	8
GND	Negative power supply	21	9
POL_RX2	Schmitt-triggered digital input that sets the polarity of the receiver RX2. To be connected to **GND** for non-inverting output or to **PVDD** for inverting output.	22	↓
POL_TX2	Schmitt-triggered digital input sets the polarity of the transmitter TX2. To be connected to **GND** for non-inverting input or to **PVDD** for inverting input.	23	↓
FR_TRIM2	Schmitt-triggered digital input control bits for oscillator frequency configuration (MSB=**FR_TRIM2**, LSB=**FR_TRIM0**). High Carrier Frequency = 22MHz with **FR_TRIM**<2:0> = "000".	24	↓
FR_TRIM1		25	↓
FR_TRIM0		26	↓
TX2_N	Negative differential output of transmitter TX2. To be connected to the primary of the pulse transformer.	27	10
TX2_P	Positive differential output of transmitter TX2. To be connected to the primary of the pulse transformer.	28	11

[1] Arrows indicate if the pin is internally pulled up (↑) or down (↓) for the given packaging option

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **PVDD-GND**	3.3		5.5	V
Voltage on all other pins[1]	GND-0.5		PVDD	V
Junction Temperature[2] T_j	-60		230	°C

[1] During transient operation, TX1_P/N, TX2_P/N and RX1_P/N, RX2_P/N can reach values under 0V and above VDD. Extreme values are limited by internal clamping diodes to GND and to VDD.

[2] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for PVDD-GND=5V, case temperature T_c in range -60°C≤T_c≤230°C or typical at T_c =85°C.

Parameter	Condition		Min	Typ	Max	Units
Supply voltage						
PVDD-GND			3.3		5.5	V
Supply current (2 TX/RX channel)						
Quiescent current I_q	TX_EN="0" and RX_EN="0" at 230°C (worst case)			45	100	µA
Duty cycle=0% I_{VDD_0}	INx="0",	1 TX + RX path FR_TRIM="000", POL_TXx="0" C_{OUTx}=70pF, at T_c=230°C (worst case)		0.8	1.5	mA
Duty cycle=50% I_{VDD_50}	INx=1MHz			5.4	9	mA
Duty cycle=100% I_{VDD_100}	INx="1"			9.6	15	mA
Dynamic specifications						
Maximum data rate	FR_TRIM<2:0> = "111" FR_TRIM<2:0> = "000"		0.7 2.5	1.2 4.2		Mbps
Modulation frequency	For all FR_TRIM<2:0> control signals			5.8 to 22		MHz
Modulation frequency variation	For FR_TRIM<2:0> = "111" For FR_TRIM<2:0> = "000"		-30 -40		+50 +20	%
Modulation frequency duty cycle	For FR_TRIM<2:0> = "111" For FR_TRIM<2:0> = "000"		48.5 48.5		52 58	%
Isolation performances (using appropriate pulse transformer as described in AN-00371-13)						
DC isolation (only depends on the pulse transformer)	At 2500V			10		MΩ
Transient common mode current immunity I_{CM}	dV/dt [kV/µs]=I_{CM} [mA]/C_{ww} [pF]				100	mA
TX Channel						
Pull-up Output Resistance on TX R_{ONH_TX}	Output sourcing 8mA at T_c=230°C (worst case)			19	25	Ω
Pull-down Output Resistance on TX R_{ONL_TX}	Output sinking 8mA at T_c=230°C (worst case)			17	23	Ω
V_{IH} of digital inputs			3.9	3.4		V
V_{IL} of digital inputs				1.55	1.05	V
Hysteresis				1.85		V
Propagation delay from INx to Tx	At T_c=-60°C (worst case) FR_TRIM<2:0> = "111" FR_TRIM<2:0> = "000"			185 72	230 110	ns
Jitter (RMS cycle-2-cycle)	For FR_TRIM<2:0> = "111" For FR_TRIM<2:0> = "000"			±85 ±25		ns
RX Channel						
Propagation delay from rising Rx to OUT	POL_RX=0 POL_RX=1		65 20	77 37	100 60	ns
Propagation delay from falling Rx to OUT	POL_RX=0 POL_RX=1		60 90	74 120	95 155	ns
V_{OH} of digital outputs OUTx	DUT sourcing 8mA at T_c=230°C (worst case)		4.5	4.75		V
V_{OL} of digital outputs OUTx	DUT sinking 8mA at T_c=230°C (worst case)			0.22	0.50	V

TYPICAL PERFORMANCE

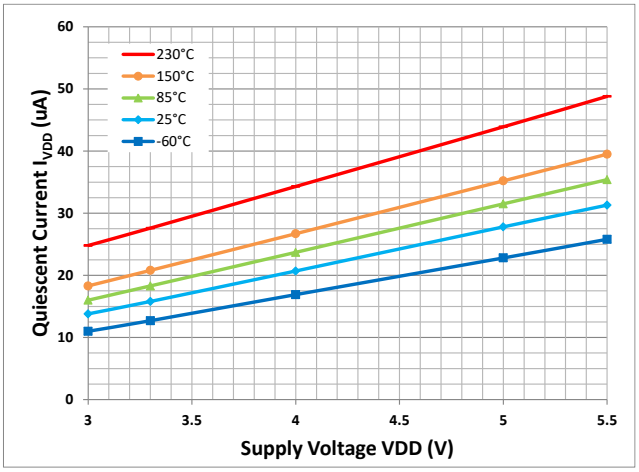


Figure 1. Quiescent Current versus supply voltage for different case temperatures.
TX_EN="0" and RX_EN="0".

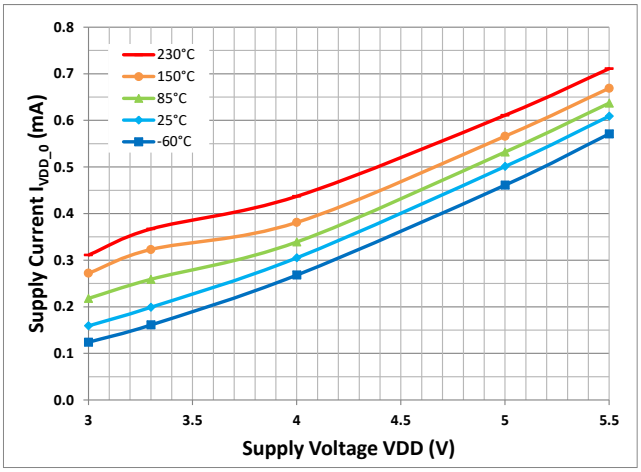


Figure 2. Consumption at DTC=0% versus supply voltage for different case temperatures. FR_TRIM="111",
INx="0", POL_xxx="0", C_{OUT}=70pF.

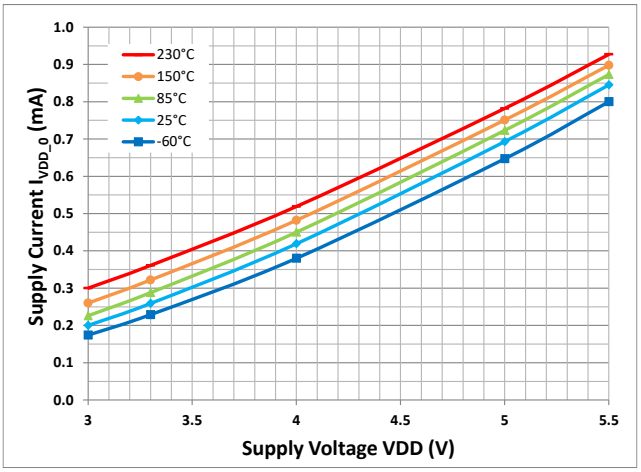


Figure 3. Consumption at DTC=0% versus supply voltage for different case temperatures. FR_TRIM="000",
INx="0", POL_xxx="0", C_{OUT}=70pF.

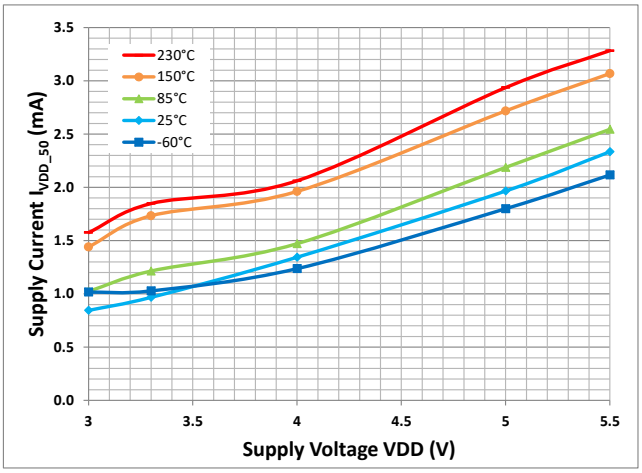


Figure 4. Consumption at DTC=50% versus supply voltage for different case temperatures. FR_TRIM="111",
IN1=1MHz with DTC=50%, IN2="0", POL_xxx="0", C_{OUT}=70pF.

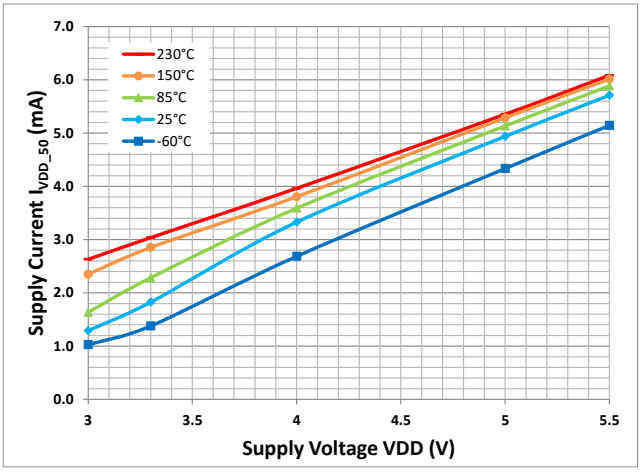


Figure 5. Consumption at DTC=50% versus supply voltage for different case temperatures. FR_TRIM="000",
IN1=1MHz with DTC=50%, IN2="0", POL_xxx="0", C_{OUT}=70pF.

TYPICAL PERFORMANCE (CONTINUED)

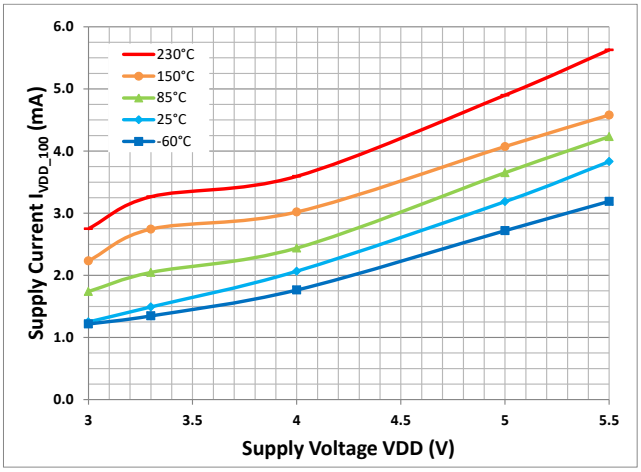


Figure 6. Consumption at DTC=100% versus supply voltage for different case temperatures. FR_TRIM="111", IN1="1", IN2="0",POL_xxx="0", C_{OUT}=70pF.

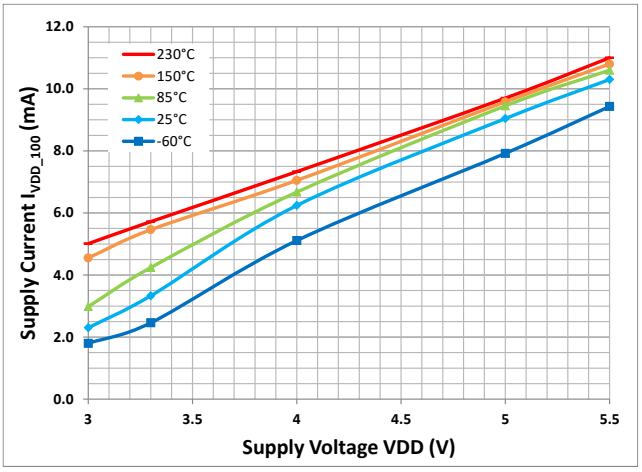


Figure 7. Consumption at DTC=100% versus supply voltage for different case temperatures. FR_TRIM="000", IN1="1", IN2="0", POL_xxx="0", C_{OUT}=70pF.

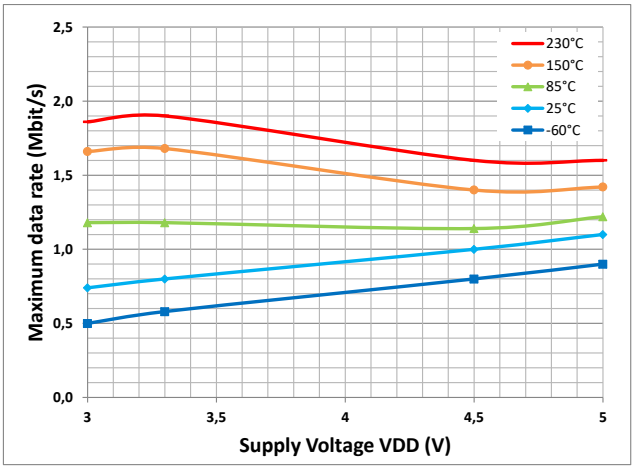


Figure 8. RX/TX maximum data rate versus supply voltage (VDD) for different case temperatures. FR_TRIM="111", C_{OUT}=70pF.

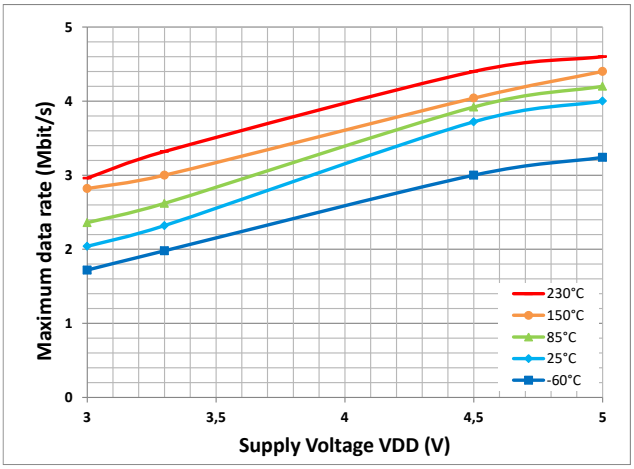


Figure 9. RX/TX maximum data rate versus supply voltage (VDD) for different case temperatures. FR_TRIM="000", C_{OUT}=70pF.

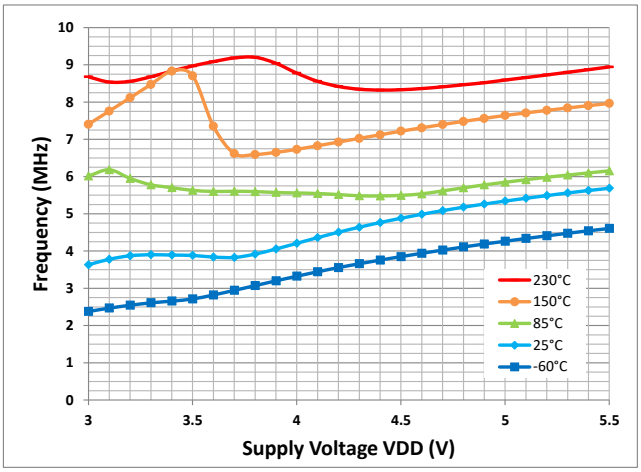


Figure 10. TX modulation frequency versus supply voltage for different case temperatures. FR_TRIM="111".

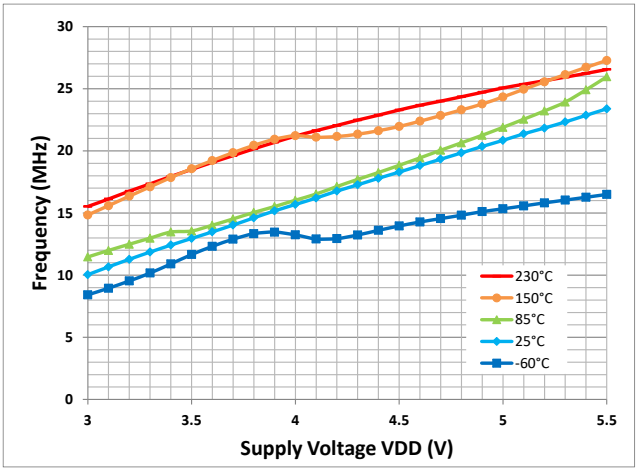


Figure 11. TX modulation frequency versus supply voltage for different case temperatures. FR_TRIM="000".

TYPICAL PERFORMANCE (CONTINUED)

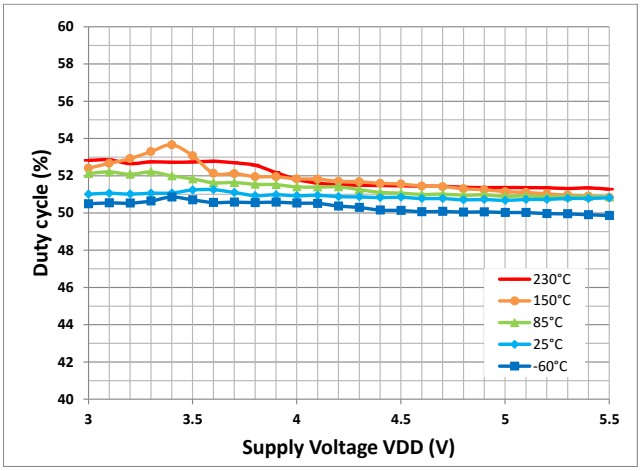


Figure 12. TX modulation duty cycle versus supply voltage for different case temperatures. FR_TRIM="111".

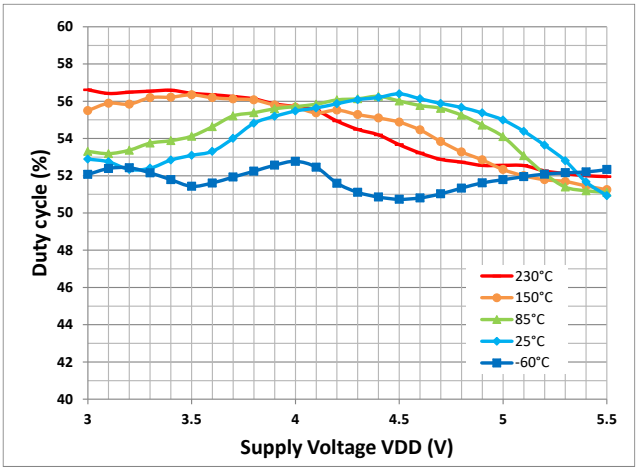


Figure 13. TX modulation duty cycle versus supply voltage for different case temperatures. FR_TRIM="000".

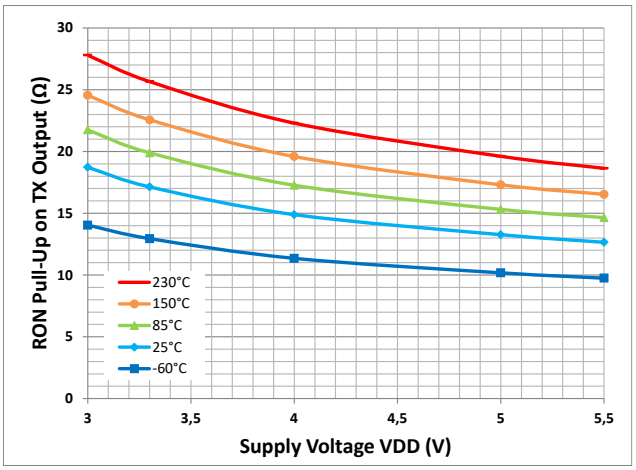


Figure 14. RON Pull-up on TX versus supply voltage for different case temperatures. Device sourcing 8 mA.

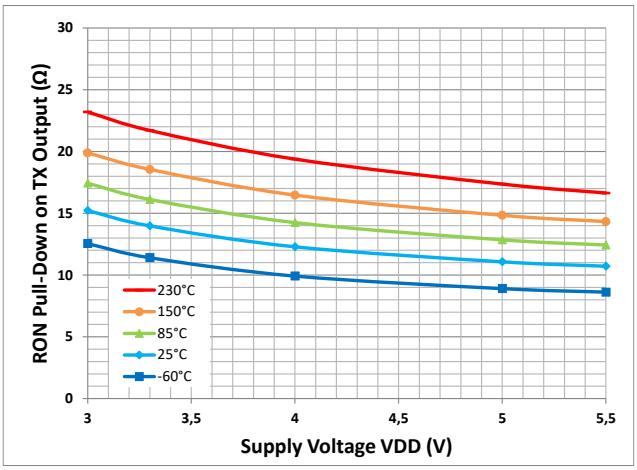


Figure 15. RON Pull-down on TX versus supply voltage for different case temperatures. Device sinking 8 mA.

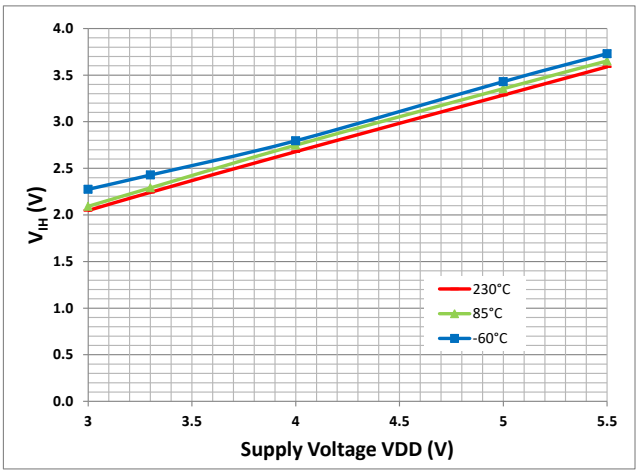


Figure 16. HIGH-level Input Voltage (V_{IH}) versus supply voltage for different case temperatures.

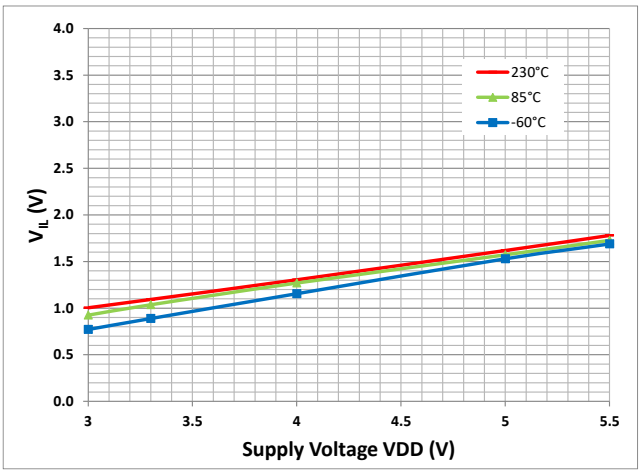


Figure 17. LOW-level Input Voltage (V_{IL}) versus supply voltage for different case temperatures.

TYPICAL PERFORMANCE (CONTINUED)

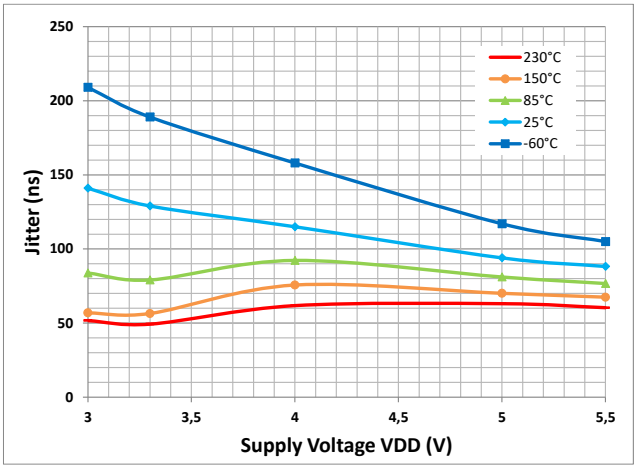


Figure 18. TX jitter versus supply voltage for different case temperatures. FR_TRIM="111".

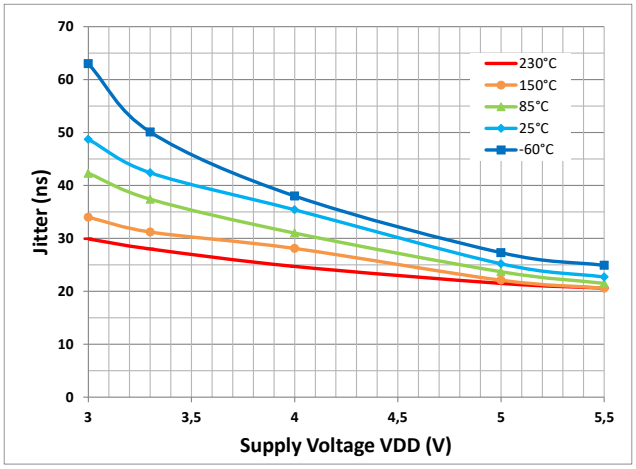


Figure 19. TX jitter versus supply voltage for different case temperatures. FR_TRIM="000".

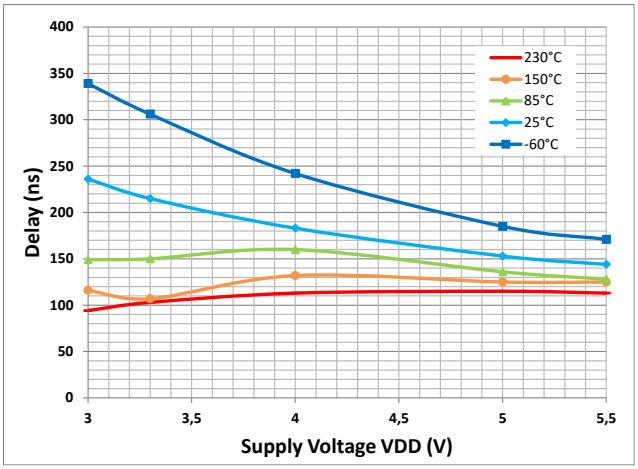


Figure 20. Delay from IN to TX versus supply voltage for different case temperatures. FR_TRIM="111".

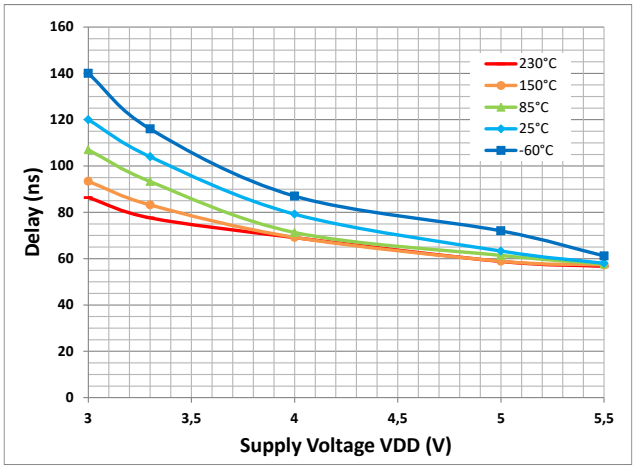


Figure 21. Delay from IN to TX versus supply voltage for different case temperatures. FR_TRIM="000".

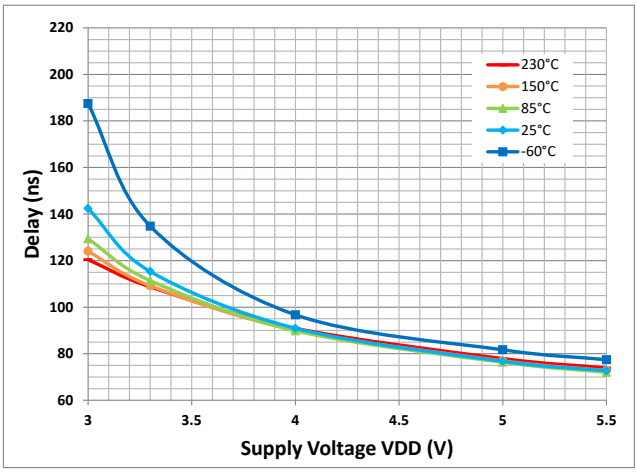


Figure 22. Delay from rising RX to rising OUT versus supply voltage for different case temperatures. POL_RXx = "0".

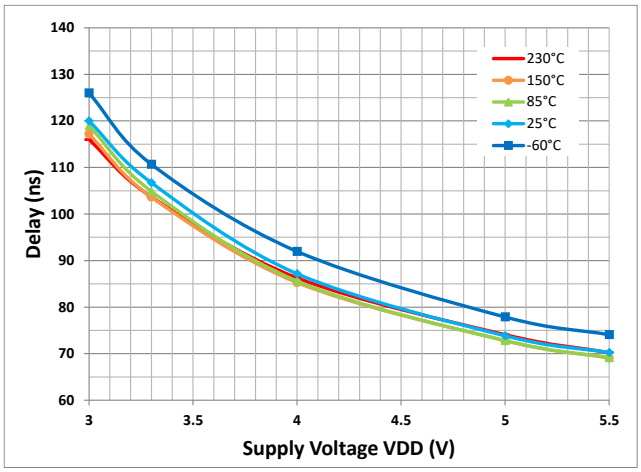


Figure 23. Delay from falling RX to falling OUT versus supply voltage for different case temperatures. POL_RXx = "0".

TYPICAL PERFORMANCE (CONTINUED)

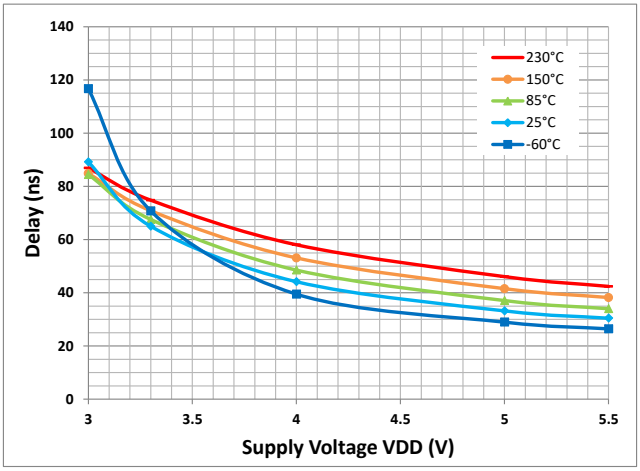


Figure 24. Delay from rising RX to falling OUT versus supply voltage for different case temperatures. POL_RXx = “1”.

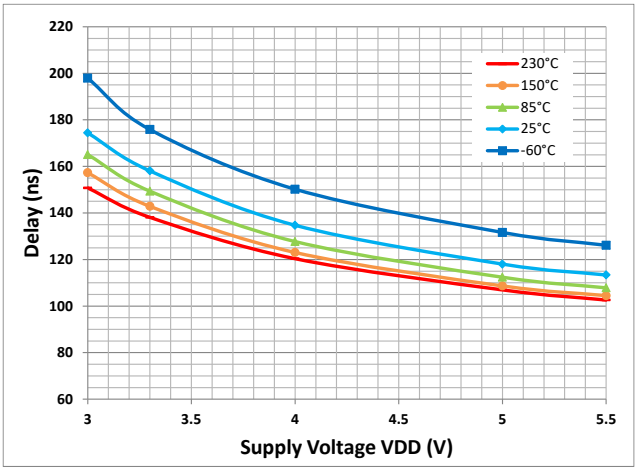


Figure 25. Delay from falling RX to rising OUT versus supply voltage for different case temperatures. POL_RXx = “1”.

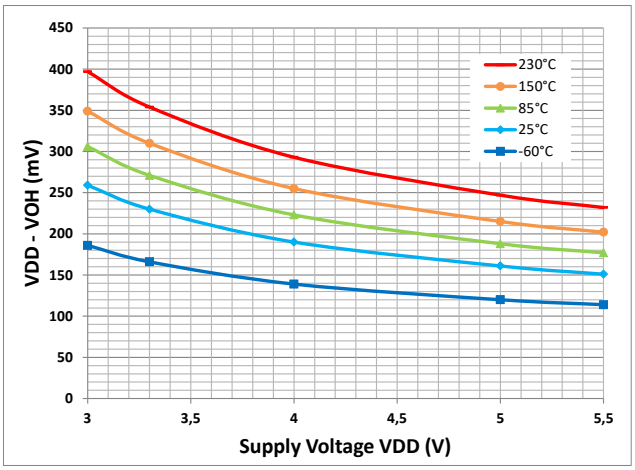


Figure 26. HIGH-level Output Voltage (V_{OH}) on OUTx versus. supply voltage for different case temperatures and I_{OUT}=8mA sinking.

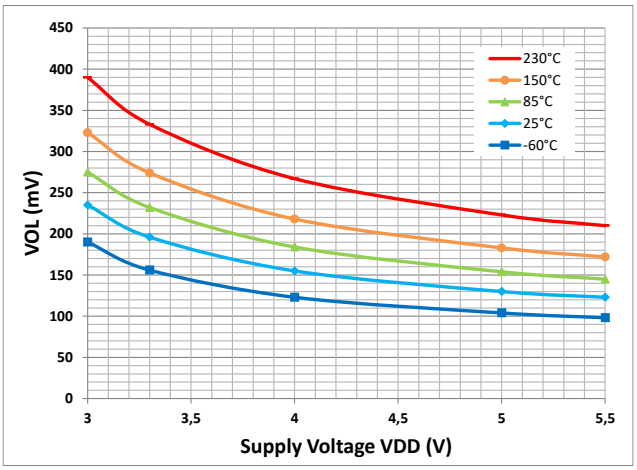


Figure 27. LOW-level Output Voltage (V_{OL}) on OUTx versus. supply voltage for different case temperatures and I_{OUT}=8mA sourcing.

THEORY OF OPERATION

Introduction

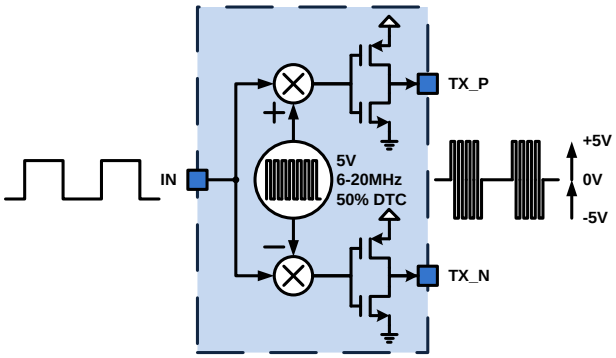
The XTR40010 implements 2 Full-Duplex Channels data transceiver. It can be used in any application where there is a need to galvanically isolate a digital data line. The galvanic isolation is achieved by an external magnetic transformer for each digital signal. The XTR40010 integrates in a single package 2 transceivers (2 TX/RX channels).

The implementation of 2 isolated full duplex TX/RX channels requires 2 XTR40010, one being connected to the primary side of the transformers and the other to the secondary side.

The XTR40010 contains 2 identical transmitters and 2 identical receivers. In the following sections, only one transmitter and one receiver will be described, and thus, the pin index 1,2 will be omitted for simplicity.

Transmitter operation

The transmitter embeds the following features to modulate the input signal with On-Off Keying modulation as shown in figure below:



- Oscillator: This block generates a clock with a 3-bits programmable frequency using the **FR_TRIM<2:0>** pins. This can be used to tune the carrier frequency to avoid EMC issues. The following table shows the typical frequency values that can be obtained:

FR_TRIM<2:0>	Carrier Frequency [MHz] @ 85°C and VDD=5V
000	21.9
001	19.7
010	18.3
011	11.3
100	10.7
101	9.4
110	8.3
111	5.8

- Modulator: This block implements a classical On-Off Keying (OOK) modulation using the clock generated by the oscillator and the digital input signal. If **POL_TX** pin is set to "0", a digital "1" at the input **IN** of the transmitter will be transferred as a differential ±5V at the output pins **TX_P/TX_N**. On the other hand, a digital "0" is transferred as a 0V versus **GND** at the output pins **TX_P/TX_N** of the transmitter. Depending on the application at system level, this behavior can be inverted by setting **POL_TX** to "1".

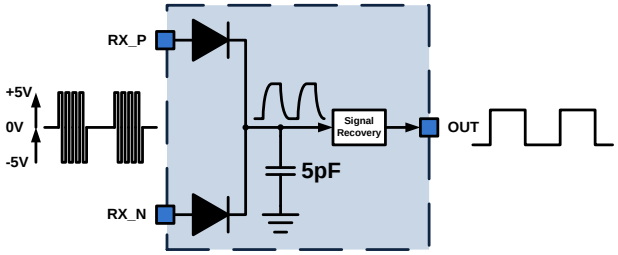
- Output buffer: it consists of several inverters with a typical R_{ON} of 10Ω for the last stage (NMOS or PMOS). This buffer is driven by two complementary signals generated by the modulator. These signals have a duty cycle very close to 50% to guarantee no DC current in the primary inductance of the pulse transformer. This DC current can induce a magnetic field that could saturate the magnetic core and compromise the data transfer.

Transmitter truth table

TX_EN	POL_TX	IN	TX_P	TX_N
0	x	x	0	0
1	0	0	0	0
1	0	1	CK	/CK
1	1	0	CK	/CK
1	1	1	0	0

Receiver operation

The receiver provides a classical full-wave rectification to demodulate the signal received on the pulse transformer secondary winding (as shown in the figure below). The signal recovery block aims to ensure immunity versus possible high dv/dt, which induces common mode current from one side of the pulse transformer to the other side. This common mode current can induce errors in the data transmission from the transmitter side to the receiver side. When a dv/dt event happens, it is detected by this block. During the dv/dt event the output data value is sustained as it was just before the dv/dt event. After the dv/dt event, the input data is transferred to the output.



Receiver truth table

EN_RX	POL_RX	RX_P	RX_N	OUT
0	x	x	x	0
1	0	0	0	0
1	0	CK	/CK	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	**forbidden**
1	1	0	0	1
1	1	CK	/CK	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	**forbidden**

Pulse transformer

The pulse transformer specifications and design guidelines are given in the application note "Pulse Transformer Design Guidelines" (AN-00371-13).

ROUTING GUIDELINES

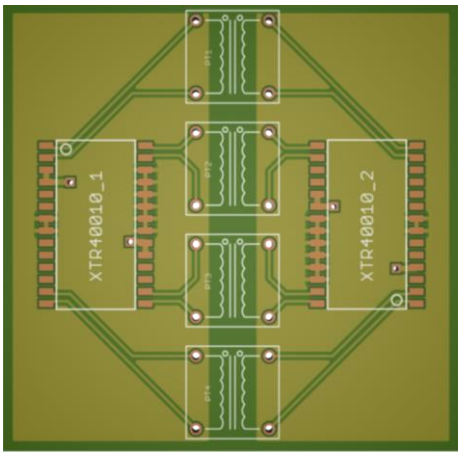
As the TX/RX signals are clocked at 20MHz with sharp transition, those signals routing from and to pulse transformers must be routed carefully. If not done, a strong coupling between different TX or RX signals may affect dV/dt immunity.

It is also recommended to set enough distance between the pulse transformers to avoid coupling between neighbors. Indeed, if there is some asymmetrical parasitic capacitive coupling between the 2 RX input traces and surrounding noisy signal traces on top of a dV/dt event, a voltage difference may occur between those RX inputs generating a false transient output state.

In addition, it is highly recommended to keep enough distance between the pulse transformers to minimize magnetic coupling between neighboring magnetic cores.

If some constraints prevent from implementing above recommendation, pull-down resistors can be added between each RX pin and VSS with value in the range of 1kΩ to 10kΩ. Also, a capacitor can be implemented between differential RX inputs. This capacitor value would be in the range of 5pF to 10pF.

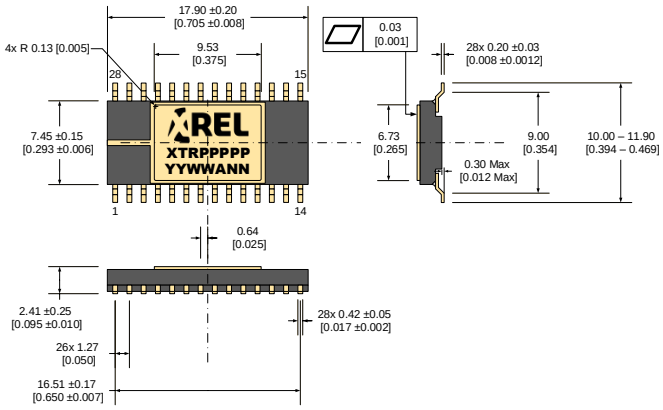
A good implementation example for a PCB routing between two XTR40010 is given hereafter:



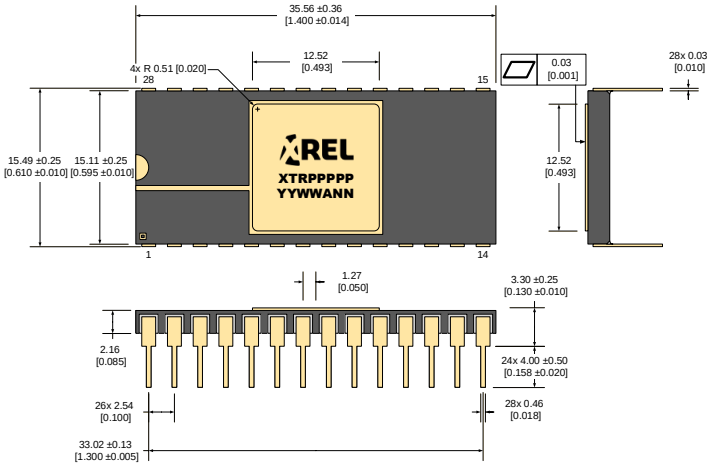
PACKAGE OUTLINES

Dimensions shown in mm [inches].

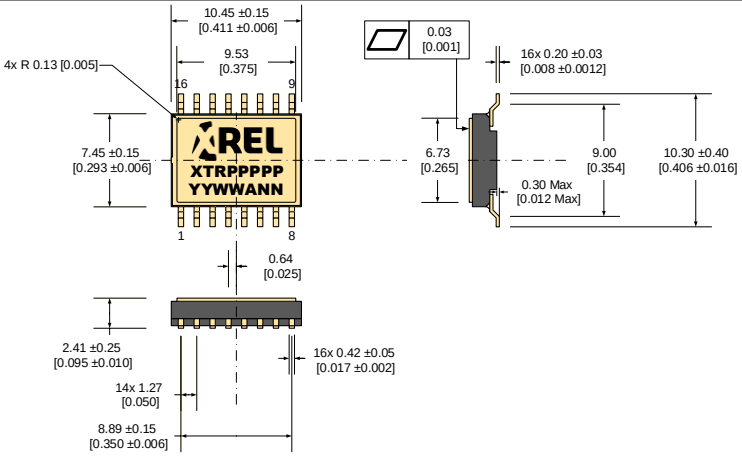
Ceramic Small Outline IC SOIC28



Ceramic Side Brazed Dual In-line DIP28



Ceramic Small Outline IC SOIC16



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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