XTR2N0500

High Temperature 35V P-Channel Power MOSFET

Rev 4 – August 2021 (DS-00150-12)

Data Sheet

PRODUCTION

CDIP8
XTR2N0525

CDFP8
XTR2N0525

FEATURES

- Minimum BV_{DSS} =-40V.
- Allowed V_{GS} range –5.5V to +5.5V.
- Operational beyond the -60°C to +230°C temperature range.
- Low $R_{DS(on)}$
  - XTR2N0525: 2.3 Ω @ 230°C
  - XTR2N0550: 1.1 Ω @ 230°C
- Maximum Peak I_D:
  - XTR2N0525: 5.3 A @ 230°C
  - XTR2N0550: 11.7 A @ 230°C
- On-time ($t_{d(on)}$+t_r):
  - XTR2N0525: 26 nsec @ 230°C
  - XTR2N0550: 31 nsec @ 230°C
- Off-time ($t_{d(off)}$+t_f):
  - XTR2N0525: 76 nsec @ 230°C
  - XTR2N0550: 91 nsec @ 230°C
- Ruggedized 3-lead TO257, 8-lead side brazed DIP and 8-lead gull-wing flat pack with ePAD.
- Also available as tested bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- DC/DC converters, power switching, motor control, power inverters, power linear regulators, power supply.

DESCRIPTION

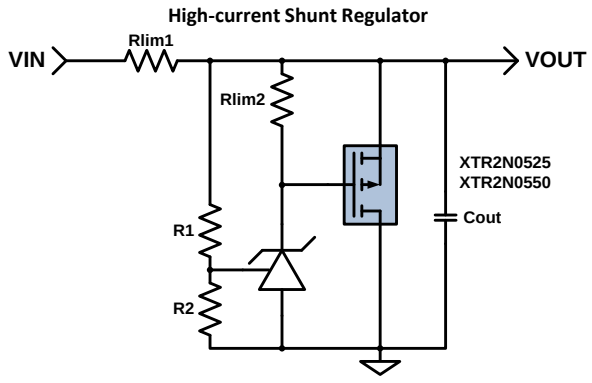
XTR2N0500 is a family of 35V P-channel power MOSFETs designed to reliably operate over a wide range of temperatures. Full functionality is guaranteed from -60°C to +230°C, though operation well below and above this temperature range is achieved.

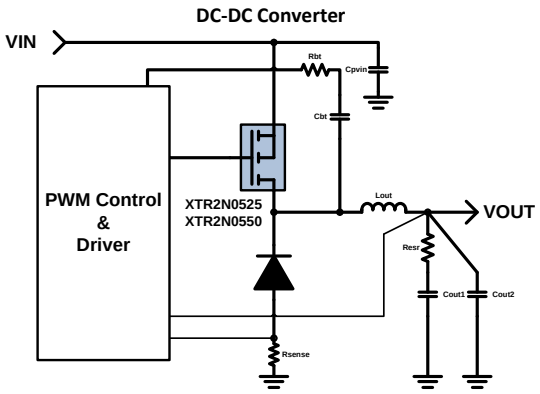
Fabricated in a Silicon-on-Insulator (SOI) process, XTR2N0500 family parts offer reduced leakage currents while providing high drain currents and low $R_{DS(on)}$. These features allow XTR2N0500 parts to be ideally suited for switching and linear applications.

XTR2N0500 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

Parts from the XTR2N0500 family are available in ruggedized 8-lead side brazed DIP and 8-lead gull-wing flat pack with ePAD. Parts are also available as tested bare die.

PRODUCT HIGHLIGHT





ORDERING INFORMATION

X	TR	2N	05xx
Source : X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR2N0525-TD	-60°C to +230°C	Tested bare die		
XTR2N0525-D	-60°C to +230°C	Ceramic side brazed DIP	8	XTR2N0525
XTR2N0525-FE	-60°C to +230°C	Gull-wing flat pack with ePad	8	XTR2N0525
XTR2N0550-TD	-60°C to +230°C	Tested bare die		

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

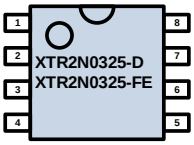
ABSOLUTE MAXIMUM RATINGS

Drain-source voltage	-40V to +2V
Gate-source voltage	±6.0V
Storage temperature range	-70°C to +230°C
Operating junction temperature range	-70°C to +300°C
ESD classification	2kV HBM MIL-STD-750

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS

DIP8 / CDFP8
Top view



1, 2, 3	**SOURCE**
4	**GATE**
5, 6, 7, 8	**DRAIN**
ePAD of CDFP8	**SOURCE**

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR2N0525-D (DIP8)					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$			20		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$	Still air.		100		°C/W
XTR2N0525-FE (DFP8 with exposed pad)					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$	Measured on ePAD.		7		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$	ePAD thermally connected to 3cm² PCB copper		70		°C/W

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Drain-source voltage V_{DS}	-35		1.5	V
Gate-source voltage V_{GS}	-5.5		+5.5	V
Junction Temperature[1] T_j	-60		230	°C

[1] *Operation beyond the specified temperature range is achieved. The -60°C to +230°C range for the case temperature is considered for the case where $I_D \leq I_{D(DC)}$ for a given case temperature.*

XTR2N0525 SPECIFICATIONS

Unless otherwise stated, specification applies for -60°C<T_J<230°C.

Parameter	Condition	Min	Typ	Max	Units
DC Characteristics					
Drain-source breakdown voltage **BV_{DSS}**	V_{GS}=0V, I_{DS}=-100μA	-40			V
Static drain-source on-state resistance **$R_{DS(on)}$**	V_{GS}=-5V, I_{DS}=-100mA T_C=-60°C T_C=85°C T_C=230°C		1.1 1.6 2.3	1.5 2.1 3.0	□
Continuous drain current **$I_{D(DC)}$**	V_{GS}=-5V T_J =-60°C T_J =85°C T_J =230°C	-1.5 -1.1 -0.9	-2.2 -1.6 -1.3		A
Gate threshold voltage **$V_{GS(th)}$**	V_{DS}=V_{GS}, I_{DS}=-1mA T_C=-60°C T_C=85°C T_C=230°		-1.27 -0.98 -0.60		V
Temperature drift of gate threshold voltage **$\Delta V_{GS(TH)}/\Delta T_j$**	V_{DS}=V_{GS}, I_{DS}=-1mA		2.31		mV/°C
Off-state drain current **I_{DSS}**	V_{DS}=-35V, V_{GS}=0V T_C=85°C T_C=230°C		-0.35 -45	-10 -200	μA
Gate leakage current **I_{GSS}**	V_{GS}=±5V, V_{DS}=0V T_C=85°C T_C=230°C		±0.6 ±170	±5 ±1000	nA
AC Characteristics					
Input capacitance **C_{iss}**	V_{DS}=-35V, V_{GS}=0V, f=1MHz		160		pF
Output capacitance **C_{oss}**			62		pF
Transfer capacitance **C_{rss}**			35		pF
Switching Characteristics					
Pulsed drain current **I_{DM}**	V_{DS}=-20V, $V_{GS\ sweep}$=0 to -5V, d=0.2%, □=1ms T_C=-60°C T_C=85°C T_C=230°C	-6.1 -4.5 -3.7	-8.7 -6.4 -5.3		A
Total gate charge **Q_g**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V		4.8		nC
Turn-on delay time **$t_{d(on)}$**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		9		ns
Rise time **t_r**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		17		
Turn-off delay time **$t_{d(off)}$**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		32		
Fall time **t_f**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		44		
Drain-Source Diode Characteristics					
Forward diode voltage **V_{SD_1A}**	V_{GS}=0V, I_{DS}=1A T_C=-60°C T_C=85°C T_C=230°C		1.34 1.23 1.09		V

XTR2N0550 SPECIFICATIONS

Unless otherwise stated, specification applies for -60°C<T_J<230°C.

Parameter	Condition	Min	Typ	Max	Units
DC Characteristics					
Drain-source breakdown voltage **BV_{DSS}**	V_{GS}=0V, I_{DS}=-100μA	-40			V
Static drain-source on-state resistance **$R_{DS(on)}$**	V_{GS}=-5V, I_{DS}=-100mA T_C=-60°C T_C=85°C T_C=230°C		0.50 0.73 1.10	0.65 0.95 1.40	□
Continuous drain current **$I_{D(DC)}$**	V_{GS}=-5V T_J=-60°C T_J =85°C T_J =230°C	-3.3 -2.4 -2.0	-4.8 -3.5 -2.9		A
Gate threshold voltage **$V_{GS(th)}$**	V_{DS}=V_{GS}, I_{DS}=-1mA T_C=-60°C T_C=85°C T_C=230°		-1.26 -0.96 -0.53		V
Temperature drift of gate threshold voltage **$\Delta V_{GS(TH)}/\Delta T_j$**	V_{DS}=V_{GS}, I_{DS}=-2.5mA		2.51		mV/°C
Off-state drain current **I_{DSS}**	V_{DS}=-35V, V_{GS}=0V T_C=85°C T_C=230°C		-0.75 -100	-20 -400	μA
Gate Leakage current **I_{GSS}**	V_{GS}=±5V, V_{DS}=0V T_C=85°C T_C=230°C		±0.8 ±190	±5 ±1000	nA
AC Characteristics					
Input capacitance **C_{iss}**	V_{DS}=-35V, V_{GS}=0V, f=1MHz		360		pF
Output capacitance **C_{oss}**			140		pF
Transfer capacitance **C_{rss}**			80		pF
Switching Characteristics					
Pulsed drain current **I_{DM}**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, d=0.2%, □=1ms T_C=-60°C T_C=85°C T_C=230°C	-13.4 -9.8 -8.1	-19.1 -14.1 -11.7		A
Total gate charge **Q_g**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V		11		nC
Turn-on delay time **$t_{d(on)}$**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		10		ns
Rise time **t_r**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		21		
Turn-off delay time **$t_{d(off)}$**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		38		
Fall time **t_f**	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		53		
Drain-Source Diode Characteristics					
Forward diode voltage **V_{SD_1A}**	V_{GS}=0V, I_{DS}=1A T_C=-60°C T_C=85°C T_C=230°C		1.16 1.00 0.85		V

XTR2N0525 TYPICAL PERFORMANCE

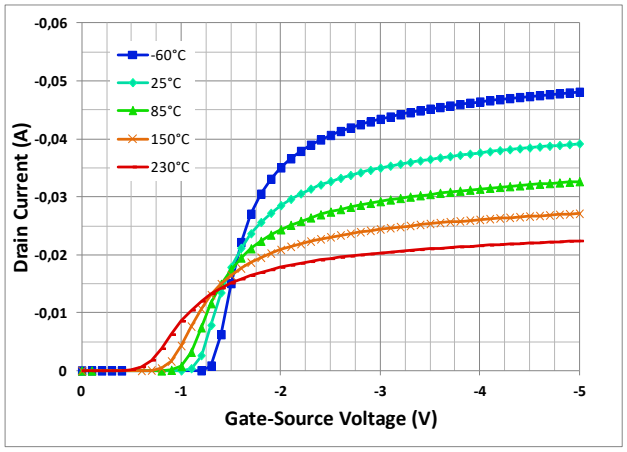


Figure 1. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

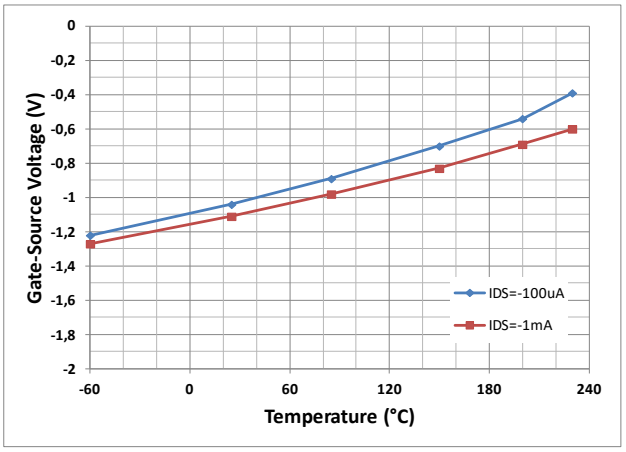


Figure 2. Gate-Source Threshold Voltage ($V_{GS(th)}$) vs Case temperatures. V_{GS}= V_{DS}.

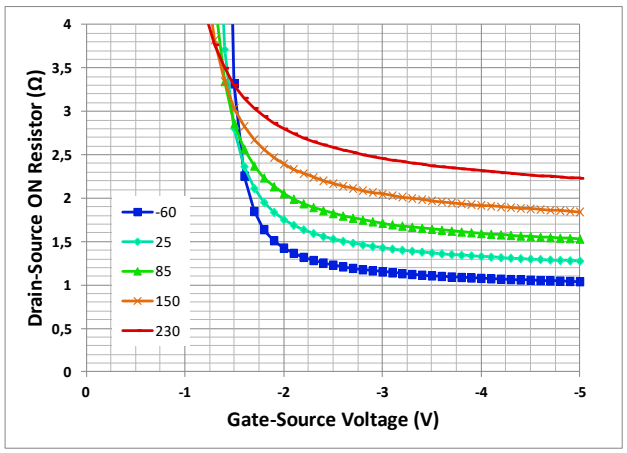


Figure 3. Drain-Source ON Resistance ($R_{DS(on)}$) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

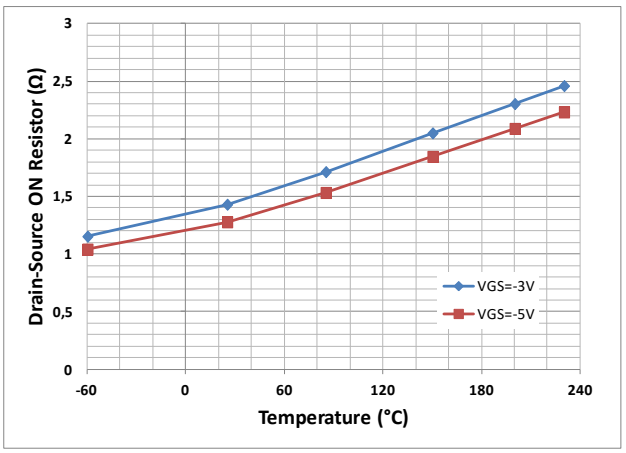


Figure 4. Drain-Source ON Resistance ($R_{DS(on)}$) vs Case Temperature. V_{DS}=-50mV.

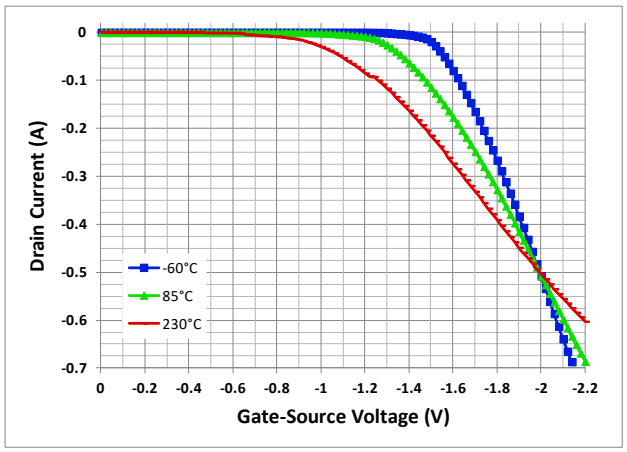


Figure 5. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{GS}=V_{DS}

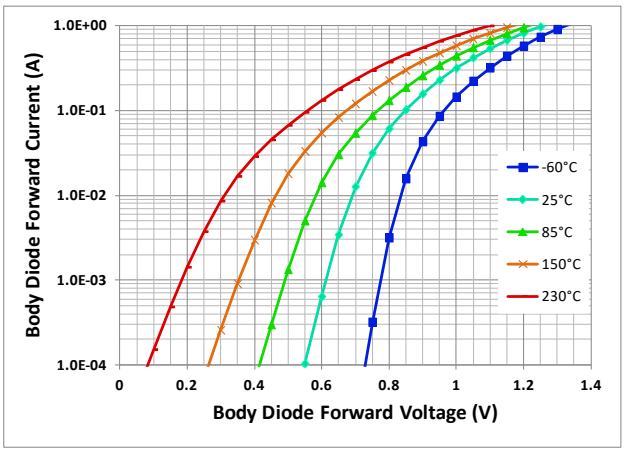


Figure 6. Body Diode Forward Current (I_{FD}) in logarithmic scale vs Forward Voltage for several case temperature. V_{GS}=0V.

XTR2N0525 TYPICAL PERFORMANCE (CONTINUED)

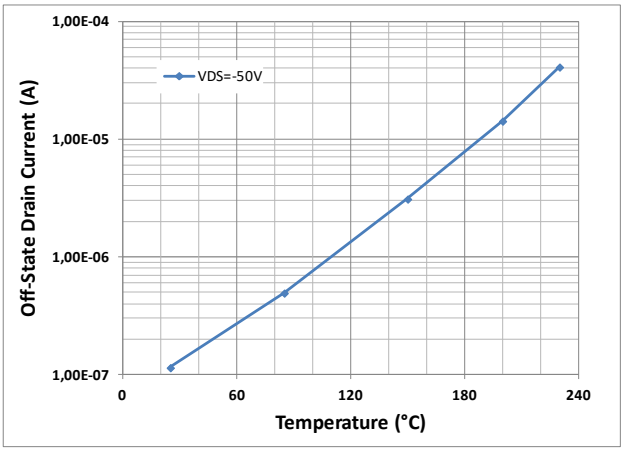


Figure 7. Off-State Drain Current (I_{DSS}) vs Case Temperature. V_{DS}=-50V, V_{GS}=0V.

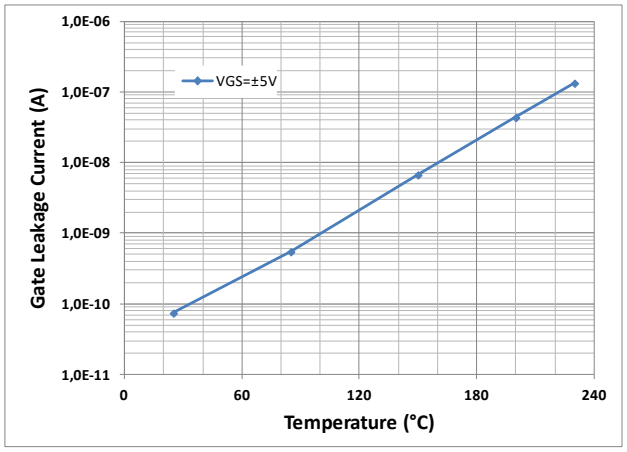


Figure 8. Gate Leakage Current (I_{GSS}) vs Case Temperature. V_{GS}=±5V, V_{DS}=0V.

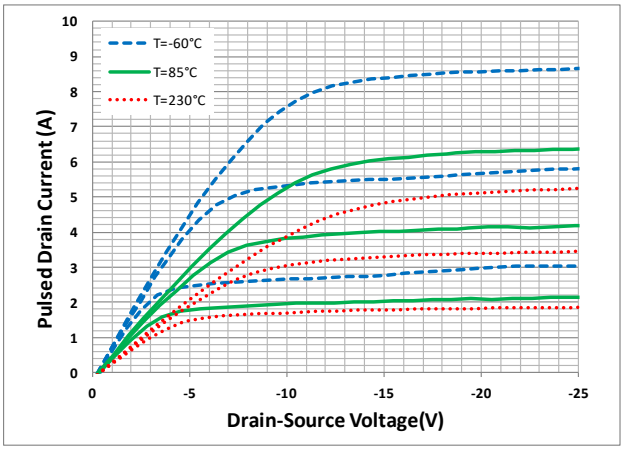


Figure 9. Pulsed Drain Current (I_{DM}) vs Drain-Source Voltage for several case temperatures. V_{GS}=-3V, -4V and -5V.

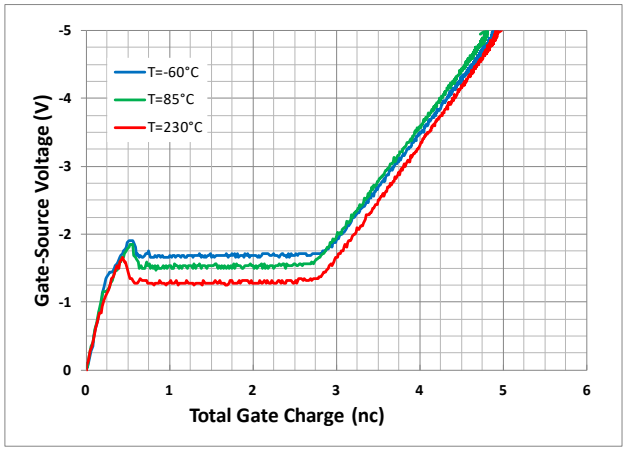


Figure 10. Total Gate Charge (Q_g) vs Gate-Source Voltage for several case temperatures. I_{DS}=-90mA.

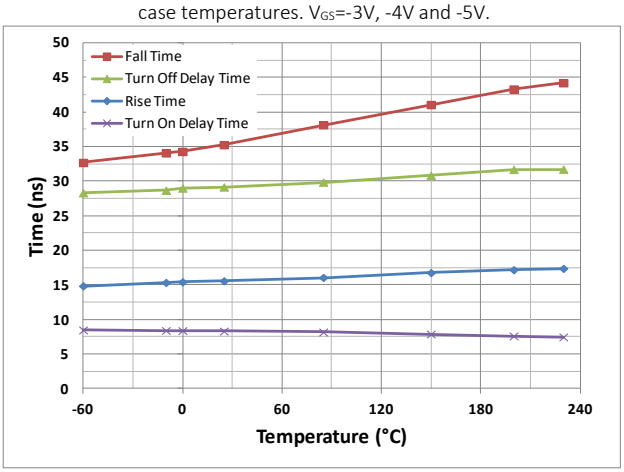


Figure 11. Timing Characteristics vs Case Temperature. V_{DS}=-25V, $V_{GS\ sweep}$= 0 to -5V.

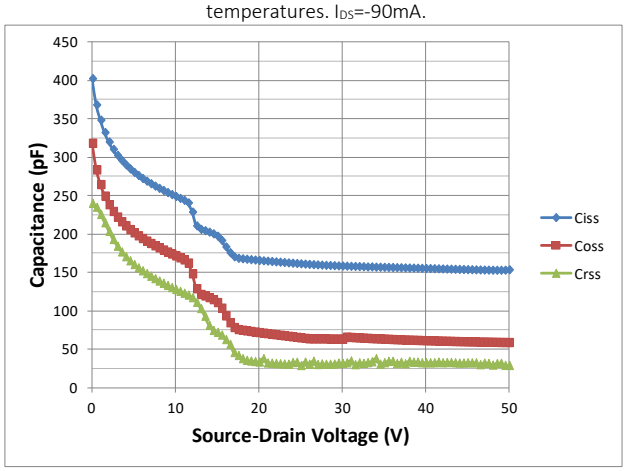


Figure 12. Capacitance vs Source-Drain Voltage at Tc=25°C.

XTR2N0550 TYPICAL PERFORMANCE

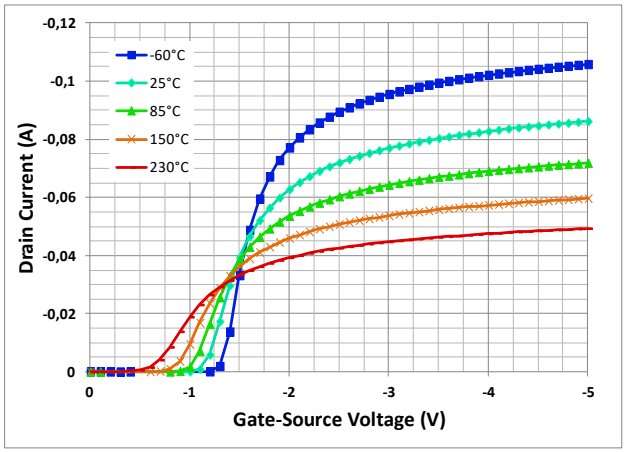


Figure 13. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

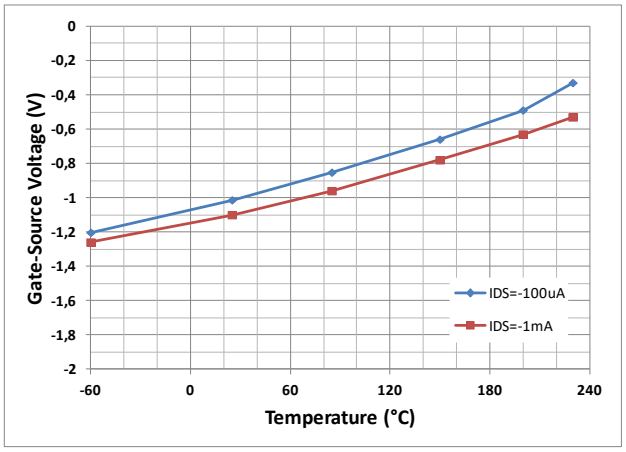


Figure 14. Gate-Source Threshold Voltage ($V_{GS(th)}$) vs Case temperatures. V_{GS}= V_{DS}.

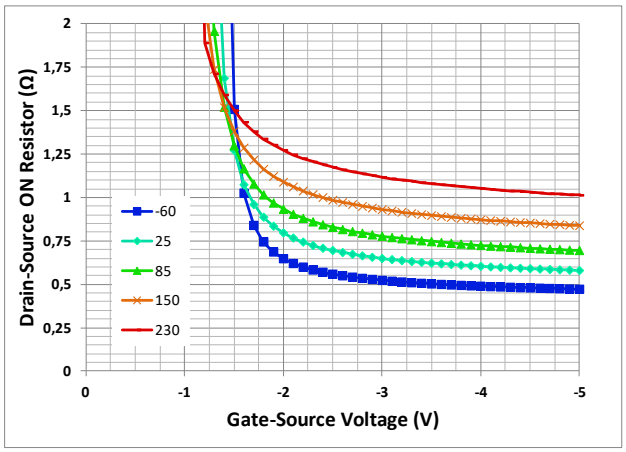


Figure 15. Drain-Source ON Resistance ($R_{DS(on)}$) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

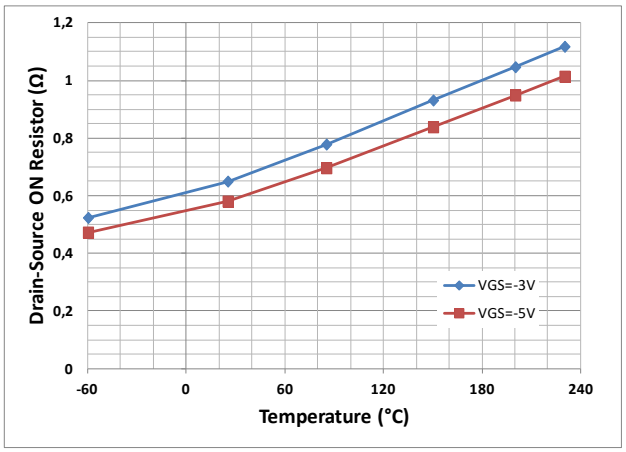


Figure 16. Drain-Source ON Resistance ($R_{DS(on)}$) vs Case Temperature. V_{DS}=-50mV.

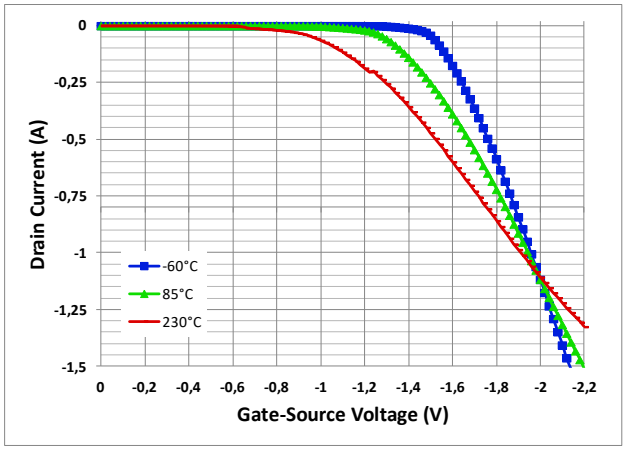


Figure 17. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{GS}=V_{DS}

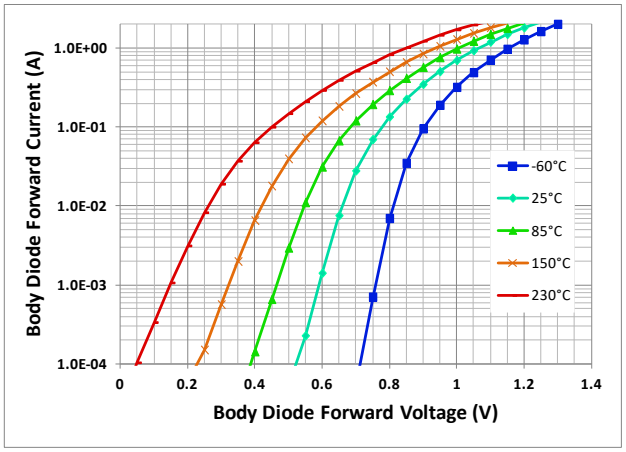


Figure 18. Body Diode Forward Current (I_{FD}) in logarithmic scale vs Forward Voltage for several case temperature. V_{GS}=0V.

XTR2N0550 TYPICAL PERFORMANCE (CONTINUED)

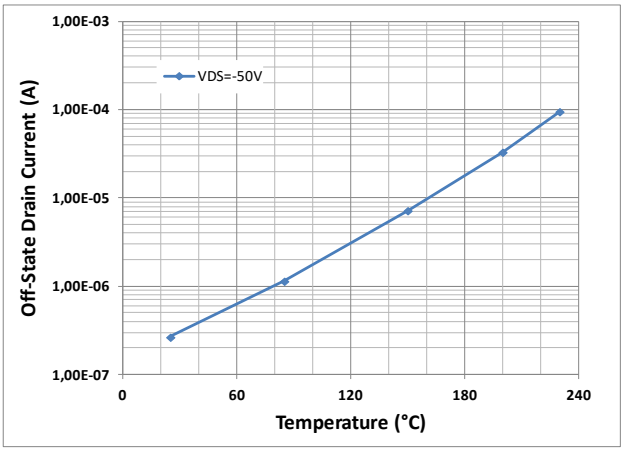


Figure 19. Off-State Drain Current (I_{DSS}) vs Case Temperature. V_{DS}=-50V, V_{GS}=0V.

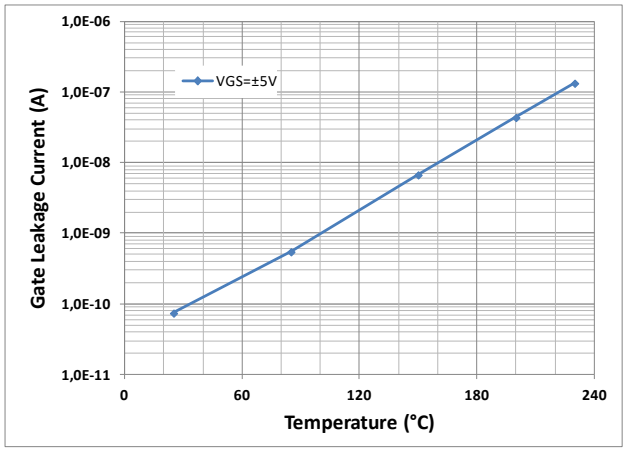


Figure 20. Gate Leakage Current (I_{GSS}) vs Case Temperature. V_{GS}=±5V, V_{DS}=0V.

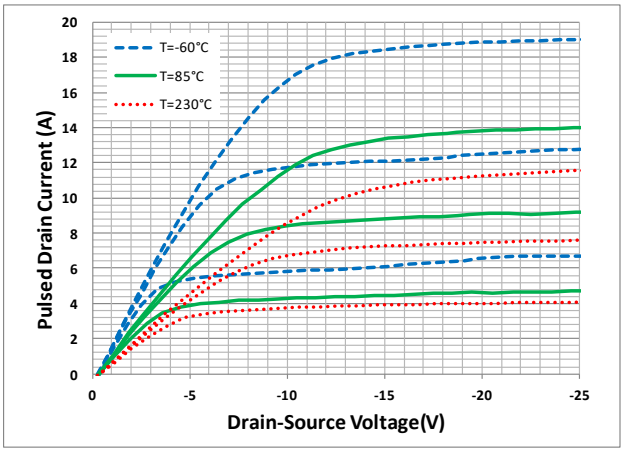


Figure 21. Pulsed Drain Current (I_{DM}) vs Drain-Source Voltage for several case temperatures. V_{GS}=-3V, -4V and -5V.

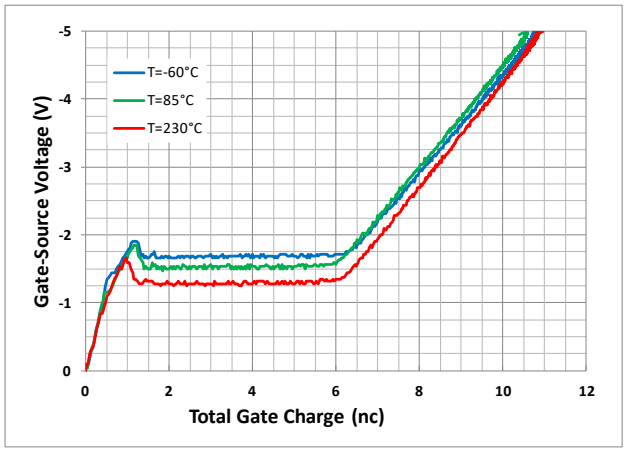


Figure 22. Total Gate Charge (Q_g) vs Gate-Source Voltage for several case temperatures. I_{DS}=-90mA.

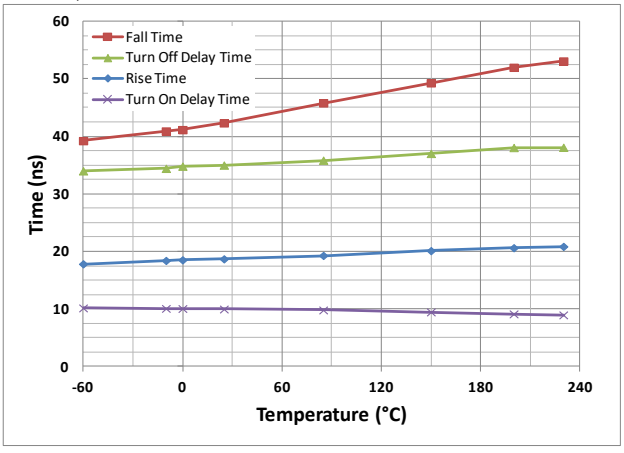


Figure 23. Timing Characteristics vs Case Temperature. V_{DS}=-25V, $V_{GS\ sweep}$= 0 to -5V.

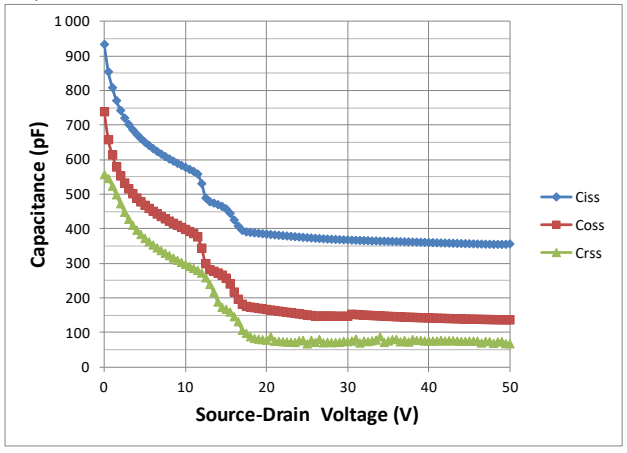


Figure 24. Capacitance vs Source-Drain Voltage at Tc=25°C.

PARAMETER DEFINITION

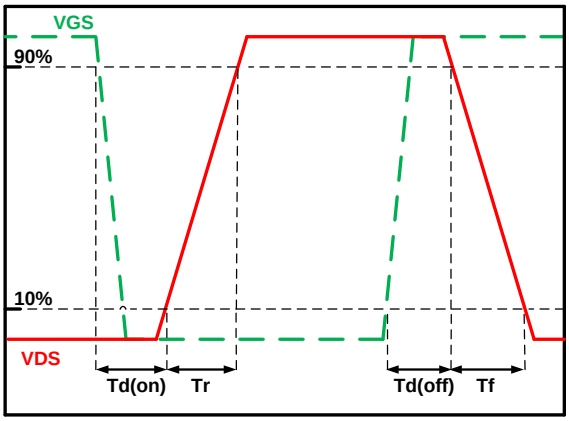
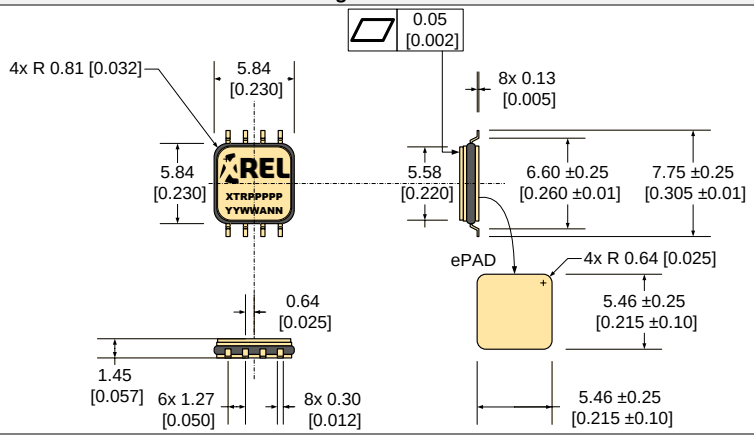


Figure 25. Timing diagram definition.

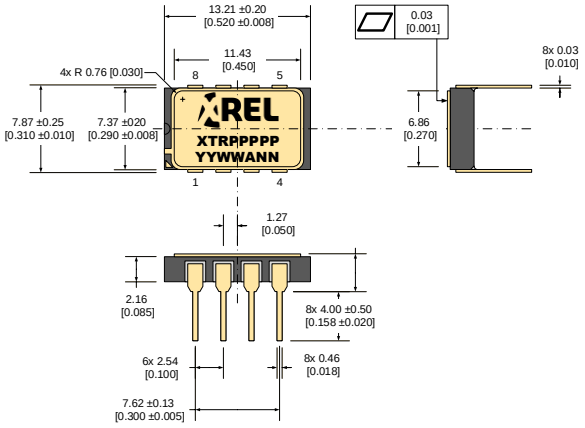
PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise stated.

Ceramic Gull-wing Flat Pack with ePad CDFP8



Ceramic Side Brazed Dual In-Line DIP8



Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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