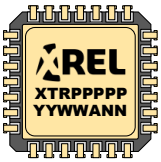
XTR26020

High Temperature Isolated Intelligent Gate Driver

Rev 3 – August 2021 (DS-00511-13)

Data Sheet

PRODUCTION



LJCC28

XTR26021

FEATURES

- Operational beyond the -60°C to +230°C temperature range.
- Supply voltage from 4.5V to 35V.
- Integrated charge-pump inside pull-up driver allowing 100% duty-cycle PWM control signal.
- Internal 5V LDO regulator.
- Safe start-up of normally-on devices.
- Isolated data transmission through multi-channel transceiver.
- Half bridge cross-conduction protection.
- Pull-up driver with 4A peak current and 1A continuous current capability at T_c=230°C.
- Pull-down driver with 2.4A peak current capability at T_c=230°C.
- On-chip active Miller clamp switch.
- Resistor-programmable under voltage lockout (ULVO).
- Resistor-programmable over-current protection level (rail-to-rail, positive and negative current sense).
- Latch-up free.
- Ruggedized SMT packages.
- Also available as bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole, Energy Conversion, Solar.
- Intelligent Power Modules (IPM).
- Motor drives.
- Uninterruptible power supplies (UPS).
- Power inverters.
- Power conversion and power factor correction (PFC).
- DC/DC converters and switched mode power supplies (SMPS).

DESCRIPTION

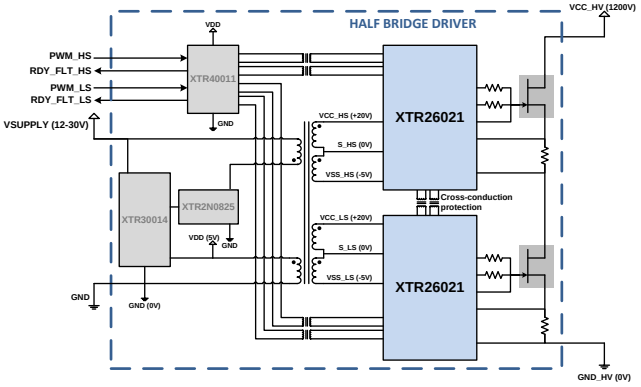
XTR26020 is a high-temperature, high reliability isolated power transistor driver designed to provide a robust, reliable, compact and efficient solution for driving a large variety of high-temperature, high-voltage, and high-efficiency power transistors. XTR26020 is able to drive normally-On and normally-Off power transistors in Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon, including JFETs, MOSFETs, BJTs, SJTs and MESFETs.

The XTR26020 driver implements unprecedented functionality for high-temperature drivers allowing safe operation at system level by preventing any cross-conduction between high-side and low-side switches, through isolated communication between high-side and low-side drivers. Other features include internal voltage regulator, 4-channel transceiver (2 TX and 2 RX) for isolated data transmission with the microcontroller and between high side and low side drivers. The XTR26020 includes one pull-up gate-drive-channel (PU_DR) capable of sourcing a typical 4A peak current and two pull-down gate-drive-channels capable of sinking a typical 2.4A peak current (PD_DR and PD_MC). The PD_DR channel is used for the effective turn-off of the power transistor, while PD_MC channel is used for Active Miller Clamping (AMC) function thanks to its internal gate level detection.

The circuit includes soft shut-down capability that slowly shuts down the power transistor in case of fault. The XTR26020 is able to detect failures due to over-current in the power switch (rail-to-rail, positive and negative current sense) or to UVLO detected on the power supply. In addition, safe start-up and cross-conduction protection are implemented to guarantee safe operation at system level.

The XTR26020 can be used standalone but also as a controller with multiplied drive capabilities using the XTR25020, which is the driver part of the XTR26020 without the isolation transceiver.

PRODUCT HIGHLIGHT



ORDERING INFORMATION

X	TR	26	020
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR26020-TD	-60°C to +230°C	Tested Die		
XTR26021-LJ	-60°C to +230°C	Ceramic LJCC28	28	XTR26020

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

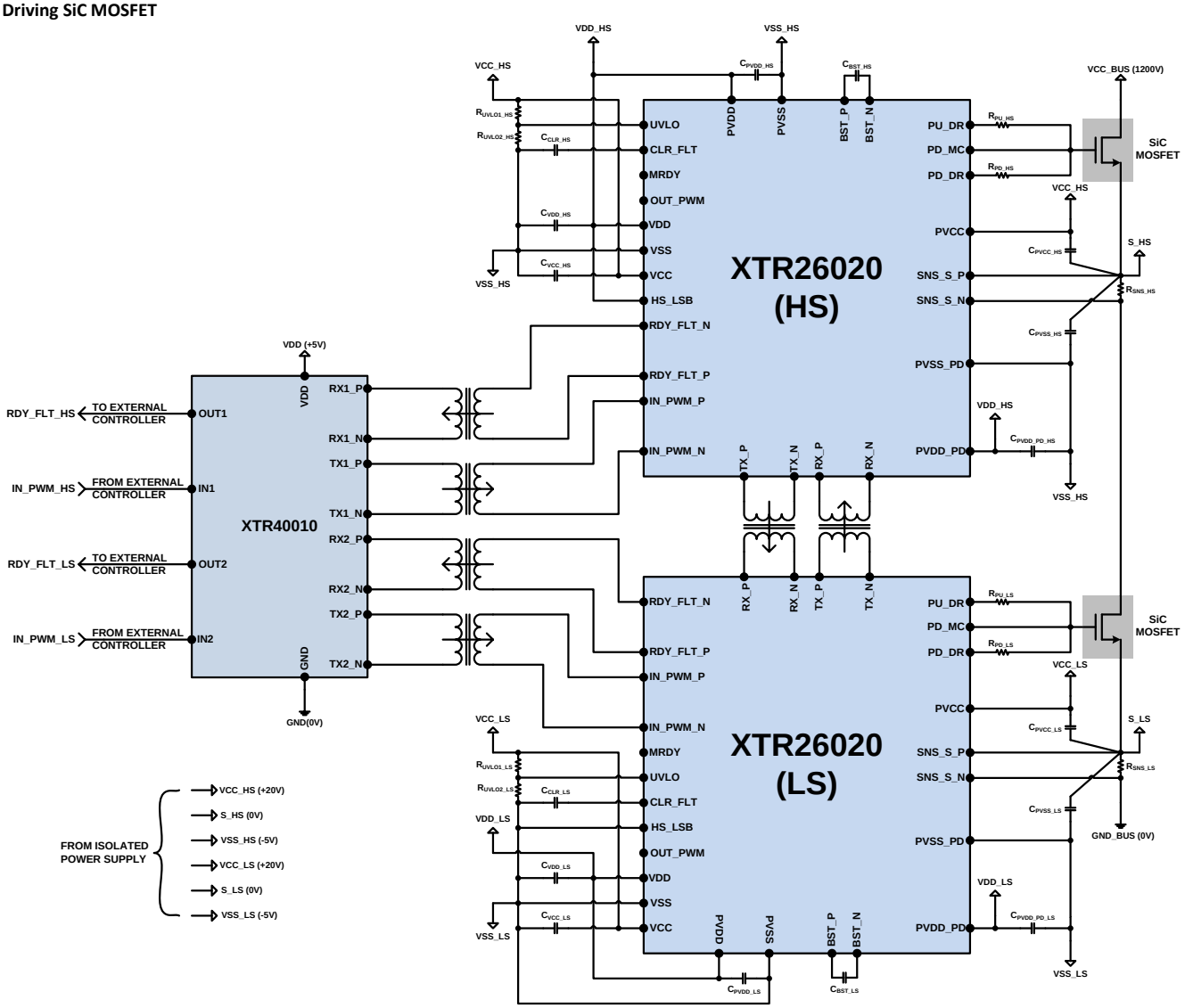
ABSOLUTE MAXIMUM RATINGS

Supply voltage:	VCC-PVSS	-0.5V to 40V
	PVCC	PVSS-0.5V to VCC+0.5V
	PVDD-PVSS	-0.5V to 5.5V
	VDD, PVDD_PD	PVSS-0.5V to PVDD+0.5V
	VSS, PVSS_PD	PVSS-0.5V to PVSS+0.5V
Inputs pins:	IN_PWM_P, IN_ PWM_N, RX_P, RX_N, HS_LSB, MRDY, CLR_FLT	PVSS-0.5V to PVDD+0.5V
	UVLO, SNS_S_P, SNS_S_N	PVSS-0.5V to VCC+0.5V
Outputs pins:	PU_DR, PD_MC, PD_DR	PVSS-0.5V to VCC+0.5V
	OUT_PWM, RDY_FLT_P, RDY_FLT_N, TX_P, TX_N	PVSS-0.5V to PVDD+0.5V
Sense pins:	SNS_S_P versus SNS_S_N	-40V to +40V
Bootstrap pins	BST_P versus BST_N	-0.5V to 6V
Storage Temperature Range		-70°C to +230°C
Operating Junction Temperature Range		-70°C to +300°C
ESD Classification		1kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

TYPICAL APPLICATION

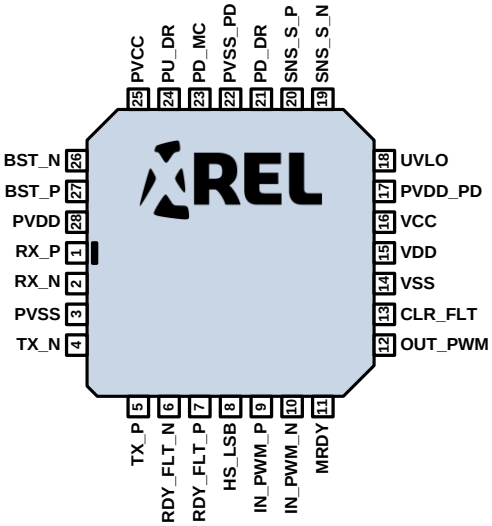
Driving SiC MOSFET



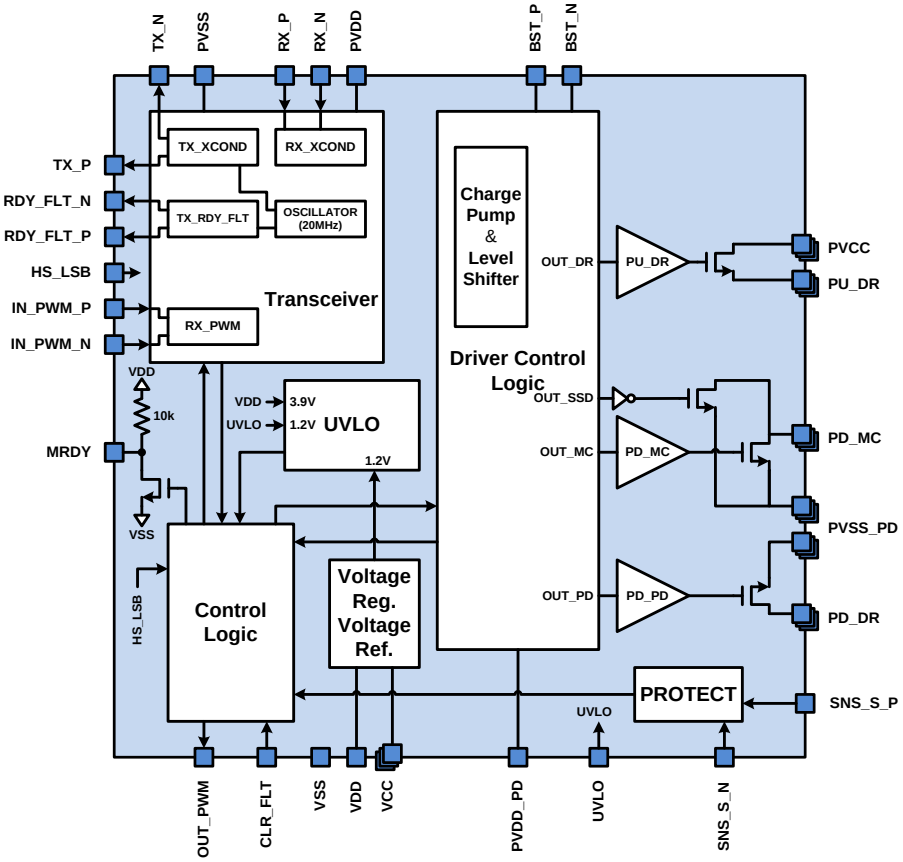
PACKAGING

J-Formed Ceramic LJCC28
XTR26021-LJ

Top view



BLOCK DIAGRAM



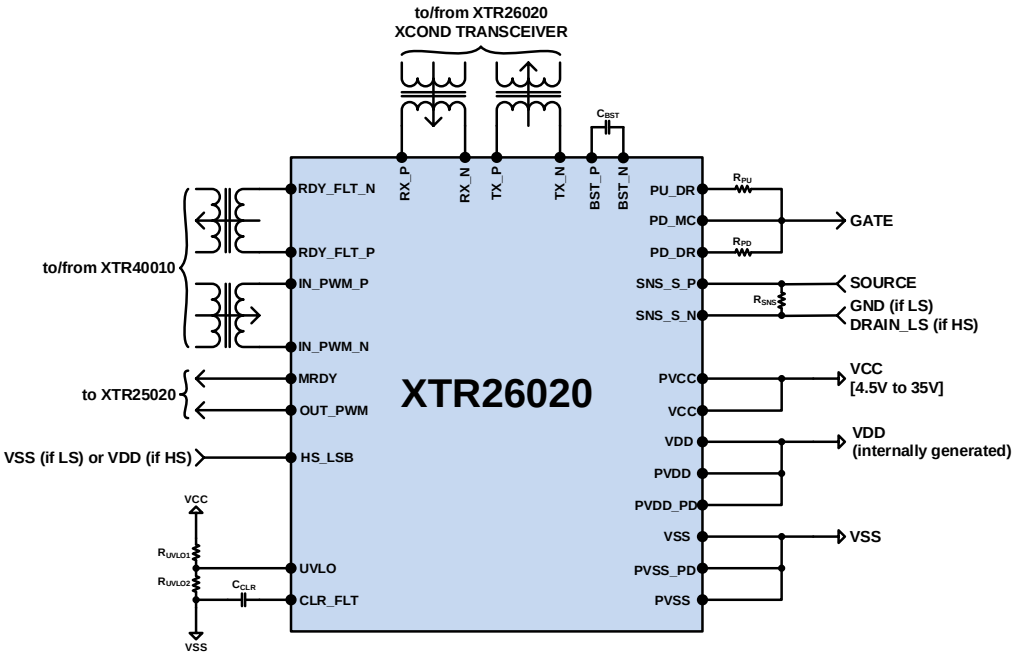
PIN DESCRIPTION

Pin number	Name	Description
1	**RX_P**	Positive input of the internal receiver of the cross-conduction information between HS and LS. If this feature is not required, connect this pin to **VDD** (**HS_LSB** must be connected to **VDD** to be in slave mode).
2	**RX_N**	Negative input of the internal receiver of the cross-conduction information between HS and LS. If this feature is not required, connect this pin to **VSS** (**HS_LSB** must be connected to **VDD** to be in slave mode).
3	**PVSS**	Negative power supply. Connect to **VSS** through a local plane.
4	**TX_N**	Negative output of the internal transmitter of the cross-conduction information between HS and LS. If this feature is not required, leave this pin floating (**HS_LSB** must be connected to **VDD** to be in slave mode).
5	**TX_P**	Positive output of the internal transmitter of the cross-conduction information between HS and LS. If this feature is not required, leave this pin floating (**HS_LSB** must be connected to **VDD** to be in slave mode).
6	**RDY_FLT_N**	Negative output giving the READY/FAULT information to the micro-controller through the isolated transceiver. If this feature is not required, leave this pin floating.
7	**RDY_FLT_P**	Positive output giving the READY/FAULT information to the micro-controller through the isolated transceiver. If this feature is not required, leave this pin floating.
8	**HS_LSB**	0/5V Schmitt triggered digital input versus **VSS** for driver operation selection as high-side (HS_LSB=1, slave mode) or low-side (HS_LSB=0, master mode).
9	**IN_PWM_P**	Positive input receiving the PWM signal from the micro-controller through the isolated transceiver. In "SLAVE" mode (i.e. **HS_LSB** pin to **VDD**) with the cross-conduction protection active, the internal PWM can be kept permanently to "1" if needed by connecting this pin to **VDD** (together with IN_PWM_N to VSS). In this specific case, no data transformer is required for the "SLAVE" part of the half bridge.
10	**IN_PWM_N**	Negative input receiving the PWM signal from the micro-controller through the isolated transceiver. In "SLAVE" mode (i.e. **HS_LSB** pin to **VDD**) with the cross-conduction protection active, the internal PWM can be kept permanently to "1" if needed by connecting this pin to **VSS** (together with **IN_PWM_P** to **VDD**). In this specific case, no data transformer is required for the "SLAVE" part of the half bridge.
11	**MRDY**	Open drain input/output giving the "ready" (when it is high) or "fault" (when it is low) information of the circuit. When the XTR26020 is used together with the XTR25020 this pin must be connected to **RDY_FLT** pin of the XTR25020. Indeed, this connection allows to synchronize "ready" or "fault" states between the two circuits to guarantee safe operation. If the XTR26020 is used alone this pin must be kept not connected.
12	**OUT_PWM**	Digital output control signal of pull-up driver PU_DR and pull-down PD_DR drivers. To be connected to **IN_PWM** pin of XTR25020 when it is used together with XTR26020. Otherwise, keep this pin not connected. Note that capacitance on this pin impacts propagation delays from IN_PWM (or RX) to PU_DR and PD_DR drivers (see functional phase theory of operation).
13	**CLR_FLT**	Connect a capacitor between this pin and **VSS** to define the clear fault time-out. If this pin is connected to VSS, the chip stays in fault until the next startup phase.
14	**VSS**	Most negative supply voltage of the driver (its value depends on the power transistor to be driven). Connect to the reference **VSS** ground plane of the circuit.
15	**VDD**	5V supply voltage versus **VSS** generated by the internal LDO and supplying all logic except the output stage of the drivers and the transceiver. Connect to a local **VDD** plane.
16	**VCC**	Positive supply voltage of the driver. This voltage must be larger than or equal to the positive supply of the output pull up driver (PVCC). Connect to **VCC** plane.
17	**PVDD_PD**	Top plate of decoupling capacitor of the pull-down (PD_DR) pre-driver. Connect to **VDD** plane.
18	**UVLO**	Sense node through external resistor divider for the UVLO on **VCC** pin versus **VSS**. Voltage on this node is compared to an internal reference of 1.2V versus **VSS**. If this feature is not required, connect this pin to **VDD** via a pull-up resistor of at least 100kΩ.
19	**SNS_S_N**	Negative sense pin of the over-current detection. Connect it to the bottom of the source or gate sense resistor using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_P** and connected to **VDD** plane.
20	**SNS_S_P**	Positive sense pin of the over-current detection. Connect it to the source or gate of the switching device, on the top of the sense resistor, using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_N** and connected to **VDD** plane.
21	**PD_DR**	Output of the pull-down driver PD_DR with a typical 2.4A peak drive current at T_c=230°C
22	**PVSS_PD**	Power **VSS** of the PD_MC driver. Connect to **VSS** plane.
23	**PD_MC**	Output of the Miller Clamp pull-down driver with a typical 2.4A peak drive current at T_c=230°C
24	**PU_DR**	Output of the pull-up driver PU_DR with typical 4A peak drive current at T_c=230°C
25	**PVCC**	Positive supply voltage of PU_DR driver. Connect to local power **PVCC** plane if different than VCC. Otherwise, connect to VCC plane.
26	**BST_N**	Negative terminal of the bootstrap capacitor of the PU_DR driver.
27	**BST_P**	Positive terminal of the bootstrap capacitor of the PU_DR driver.
28	**PVDD**	5V supply voltage versus **PVSS** supplying the transceiver, the output stage of the drivers, and the low voltage IO ring. Connect to a local power **VDD** plane.

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR260211-LJ					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$			14		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$			50		°C/W

RECOMMENDED OPERATING CONDITIONS

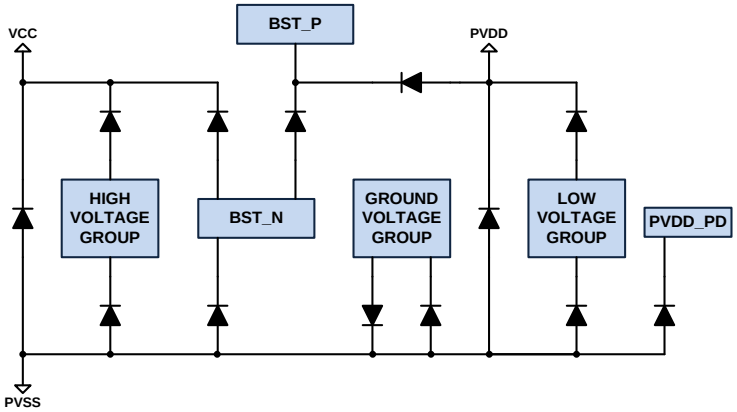


Parameter	Min	Typ	Max	Units
High voltage power supply VCC-VSS[1]	4.5		35	V
High voltage current sense inputs: SNS_S_N, SNS_S_P	VSS		VCC	
High voltage driver outputs: PU_DR, PD_DR, PD_MC	VSS		VCC	
Low voltage power supply VDD-VSS (generated from internal voltage regulator)	4.5		5.5	V
Low voltage inputs: IN_PWM_N, IN_PWM_P, HS_LSB, UVLO, MRDY, RX_P, RX_N, CLR_FLT	VSS		VDD	
Low voltage outputs: OUT_PWM, MRDY, RDY_FLT_P, RDY_FLT_N, TX_P, TX_N	VSS		VDD	
Junction Temperature[2] T_j	-60		230	°C

[1] For VCC-VSS≤5.5V, VDD must be shorted to VCC.
[2] Operation beyond the specified temperature range is achieved.

ESD CLAMPING SCHEME

Pin Groups	Pins
High voltage power supply	VCC-PVSS
High voltage group	PD_DR, PU_DR, PVCC, SNS_S_N, SNS_S_P, PD_MC, UVLO, BST_ N
Low voltage power supply	PVDD-PVSS
Low voltage group	VDD, RX_N, RX_P, TX_N, TX_P, RDY_FLT_N, RDY_FLT_P, IN_PWM_N, IN_PWM_P, CLR_FLT, HS_LSB, OUT_PWM, MRDY
Bootstrap voltages	BST_ N, BST _P
Power VDD voltage	PVDD_PD
Ground voltage group	VSS, PVSS_PD



ELECTRICAL PERFORMANCE

Unless otherwise stated, specification applies for VCC-VSS=25V and -60°C≤T_C≤230°C. Typical values are given at T_C=25°C

Parameter		Condition	Min	Typ	Max	Units
Supply Voltage						
VCC-VSS[1]			4.5		35	V
Source of the power transistor			VSS		VCC	V
Quiescent current consumption	I_{q0}	In ready mode with IN_PWM low	6	10	15	mA
	I_{q1}	In ready mode with IN_PWM high ($C_{BST=100nF}$)	6.5	11.5	17.5	mA
Dynamic current consumption I_{Dyn}		In ready mode, 1nF output capacitor IN_PWM frequency 100KHz (50% duty)	8	12.5	18	mA
Fault state current consumption I_{fault}		In fault state with CLR_FLT tied to VSS and no TX active[2]	2.5	4	7	mA
Drivers PU_DR, PD_DR, PD_MC and SSD						
ON resistance of pull-up transistor $R_{ON\_PU\_DR}$		I_{DS}=200mA		1.2	2.7	Ω
ON resistance of pull-down transistor $R_{ON\_PD\_DR}$, $R_{ON\_PD\_MC}$		I_{DS}=200mA		1.2	2.7	Ω
ON resistance Soft-shutdown transistor R_{ON_SSD}		V_{DS}=2V while OCP fault ON	40	80	200	Ω
Peak output current of PU_DR I_{Peak_PU}		100nF output capacitor	2.8	5		A
Peak output current of PD_DR or PD_MC I_{Peak_PD}		100nF output capacitor	1.8	3.3		A
Continuous output current of PU_DR I_{DC_PU}		VCC-VSS≥7V[3]		1		A
Miller Clamp activation threshold V_{TH_MC}			0.7	1	1.45	V
Internal Linear Voltage Regulator (LDO)						
Output voltage V_{DD}		VCC-VSS=25V, 1mA≤I_{LOAD}[4]≤60mA		5		V
Total accuracy		7V≤VCC-VSS≤35V, 1mA≤I_{LOAD} ≤60mA	4.75		5.25	V
		5.5V≤VCC-VSS≤7V, 1mA≤ I_{LOAD} ≤20mA	4.5		5.25	V
Load regulation $\Delta V_{DD}/\Delta I_{load}$		VCC-VSS=25V, 1mA≤I_{LOAD}≤60mA		1.35		V/A
Line regulation[5] $1/V_{DD}$. $[(\Delta^{max}V_{DD})/\Delta V_{CC})]$		7V≤VCC-VSS≤35V I_{LOAD}=60mA		±0.025		%/V
Output current (~=I_{LOAD}+I_{q0})		7V≤VCC-VSS≤35V	0		60	mA
		5.5V<VCC-VSS<7V	0		30	mA
Output load capacitance		0.01Ω≤ESR≤0.1Ω	0.33	1	3.3	µF
UVLO						
UVLO pin thresholds voltages (for UVLO on VCC or SOURCE)	$V_{TH+\_UVLO\_VCC}$	UVLO pin rising edge		1.26		V
	$V_{TH-\_UVLO\_VCC}$	UVLO pin falling edge		1.14		V
UVLO VDD thresholds voltages	$V_{TH+\_UVLO\_VDD}$	VDD UVLO rising edge		3.95		V
	$V_{TH-\_UVLO\_VDD}$	VDD UVLO falling edge		3.50		V
Allowed input current on UVLO pin		UVLO pin when clamping at about 5.7V versus. VSS.			1	mA
Leakage current on UVLO pin		1.14V≤V_{UVLO}≤1.26V			1	µA
Control Logic						
Peak output current (sink and source) on OUT_PWM pin		50pF output capacitor	10			mA
High-Level Output Voltage on OUT_PWM V_{OH_BUFF}		DUT sourcing 8mA	4	4.65		V
Low-Level Output Voltage on OUT_PWM V_{OL_BUFF}		DUT sinking 8mA		0.2	0.5	V
High-Level Input Voltage V_{IH}		Schmitt triggered input (HS_LSB)	4	3.28		V
Low-Level Input Voltage V_{IL}		Schmitt triggered input (HS_LSB)		1.72	1	V

[1] For VCC-VSS≤5.5V, pins VDD, PVDD, and PVDD_PD must be shorted to VCC.

[2] TX is not active in case HS_LSB=VDD, RX_P-RX_N=VDD

[3] The power dissipated needs to be considered when using the 26020 at its maximum continuous current capabilities.

[4] I_{LOAD} is the current sourced by the LDO to the external measurement tool. LDO is simultaneously sourcing current to internal logic (This internal current can be considered closed to I_{q0} when in ready mode with IN_PWM=0)

[5] $\Delta^{max}V_{DD}$ is the difference between the maximum and the minimum voltages VDD measured in specified VCC range at given I_{LOAD} current

Parameter		Condition	Min	Typ	Max	Units
Schmitt triggered input hysteresis				2		V
Over-current protection between SNS_S_P and SNS_S_N						
OCP sense thresholds voltages	$V_{TH+\_OCP\_pos}$[6] $V_{TH-\_OCP\_pos}$	SNS_S_P > SNS_S_N, 0 < SNS_S_N < VCC		105 95		mV
	$V_{TH+\_OCP\_neg}$ $V_{TH-\_OCP\_neg}$	SNS_S_P < SNS_S_N, 0 < SNS_S_N < VCC		-105 -95		
OCP Sense threshold voltage accuracy		For 0 ≤ SNS_S_N ≤VCC/2 and SNS_S_N = VCC	-20		+20	%
		For VCC/2 < SNS_S_N < VCC T_C=-60°C T_C=85°C T_C=230°C	 -20 -20 -20		 +40 +30 +20	%
Protections timings						
Blanking time of over current protection t_{BLANK_OCP}		Internally fixed		400		ns
Blanking time of UVLO pin protection t_{BLANK_UVLO}		Internally fixed		11		us
Clear fault time t_{CLR_FLT}		Externally set with C_{CLR}=1nF		30		µs/nF
Recommended range for clear fault time		t_{CLR_FLT}= C_{CLR} x 30µs/nF	3	30	3000	µs
Main timings						
Propagation delays	t_{IN_PWM}[7]	From IN_PWM to OUT_PWM[8]	95	115	140	ns
	t_{RX}[7]	From RX_P/N to OUT_PWM[8]	95	100	120	ns
	T_{DR_PU}	From ⅔ of OUT_PWM to PU_DR	85	140	240	ns
	T_{DR_PD}	From ⅓ of OUT_PWM to PD_DR	85	140	240	ns
Rise time[9] t_r		1nF output load capacitance Delay 10% - 90% of PU_DR	7	11	21	ns
Fall time[9] t_f		1nF output load capacitance Delay 90% - 10% of PD_DR	9	16	28	ns
Minimum ON time t_{ON_min}		Cross-conduction protection active	1			µs
		Cross-conduction protection inactive	0.5			µs
Minimum OFF time t_{OFF_min}		Cross-conduction protection active	1			µs
		Cross-conduction protection inactive	0.5			µs
Transceiver						
Carrier frequency		TX_P/N and RDY_FLT_P/N OOK modulated signals		21		MHz
Carrier duty cycle				50		%
Jitter				50		ns
Maximum data rate		For an input PWM with D=50%		2		Mbps
Common-mode current immunity (see AN-00371-13 for details)					100	mA
TX_P and TX_N output resistance (RON)		VDD=5V		15		Ω
TX_P, TX_N output buffer V_{OH_TX}		DUT sourcing 16mA	4			V
TX_P, TX_N output buffer V_{OL_TX}		DUT sinking 16mA			0.5	V

[6] See diagram in "Functional Features" section for Over-current protection threshold definitions.
[7] In graphs, the suffix "rise" and "fall" are added respectively for measurements done on rising edge or falling edge of input signal
[8] Delay in between input signal at 50% and OUT_PWM at 10% when rising, 90% when falling
[9] The rise and fall time measurement have been performed with all driver outputs shorted (PU_DRx, PD_DR_x, PD_MC_x) and connected to a load capacitance C_{LOAD}=1nF

TYPICAL PERFORMANCE

Unless otherwise stated, temperature parameter is "Case temperature" T_C
Graphical legend "VDD=VCC" means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

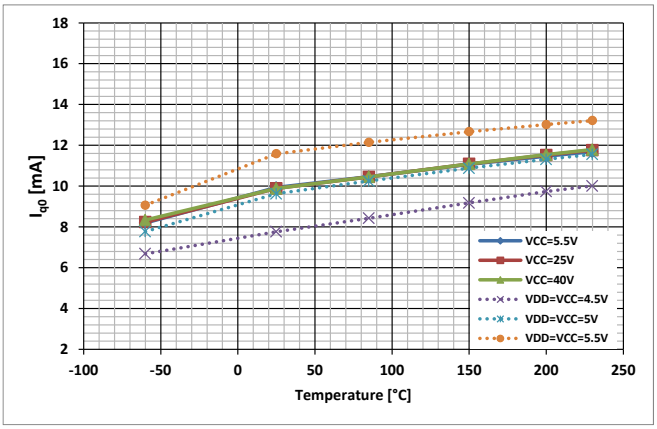


Figure 1. Quiescent current consumption I_{q0} (IN_PWM low) versus case temperature.

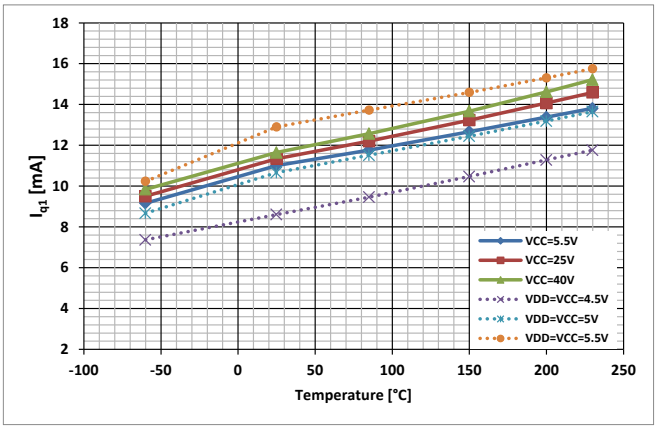


Figure 2. Quiescent current consumption I_{q1} (IN_PWM high) versus case temperature.

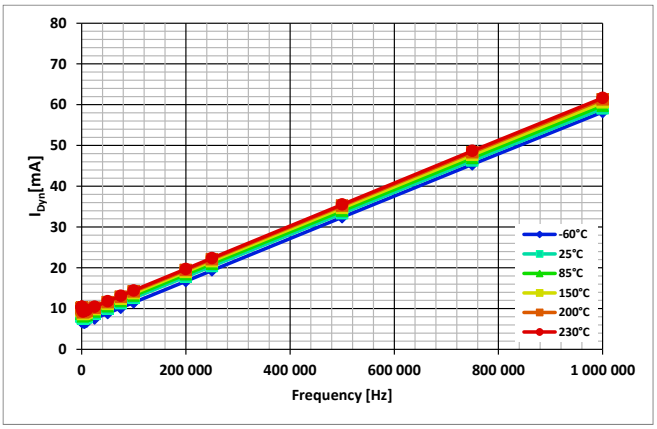


Figure 3. Dynamic consumption I_{Dyn} versus IN_PWM[10] frequency at VCC=25V (C_{LOAD}[11]=1nF, C_{BST}=100nF).

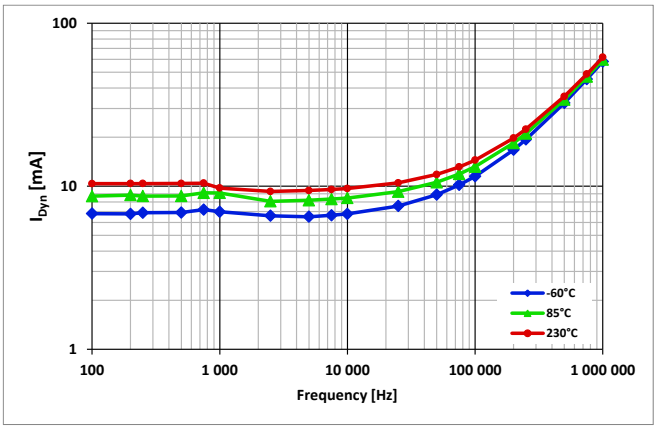


Figure 4. I_{Dyn} versus IN_PWM[10] frequency at VCC=25V (C_{LOAD}[11]=1nF, C_{BST}=100nF). Logarithmic representation.

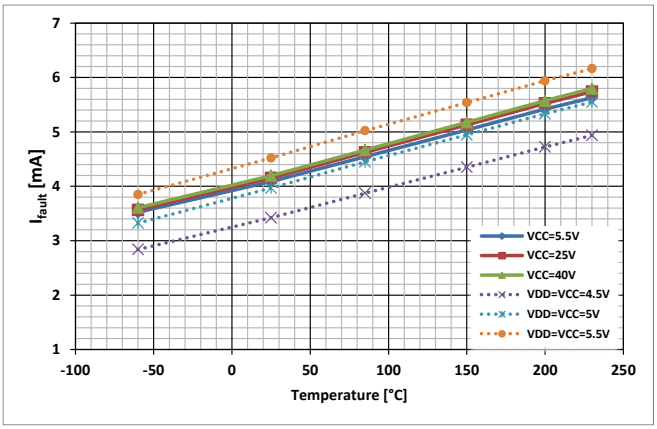


Figure 5. Fault state current consumption I_{fault} versus case temperature (same results for UVLO and OCP fault).

[10] *IN_PWM_P signal driven by a square signal (50% duty cycle) from a waveform generator, and IN_PWM_N at VSS*
[11] *C_{LOAD} is the driver outputs load capacitance including board parasitic capacitance. Drivers PU_DR, PD_DR and PD_MC are connected together.*

TYPICAL PERFORMANCE (CONTINUED)

Unless otherwise stated, temperature parameter is "Case temperature" T_C
Graphical legend "VDD=VCC" means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

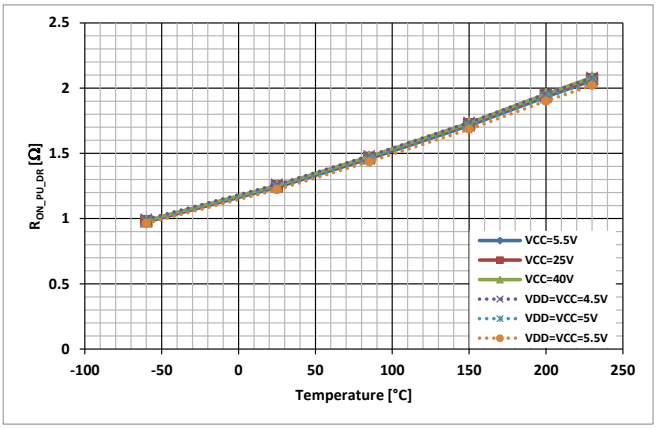


Figure 6. R_{ON} of pull-up driver (PU_DR) versus case temperature (I_{DS}=200mA).

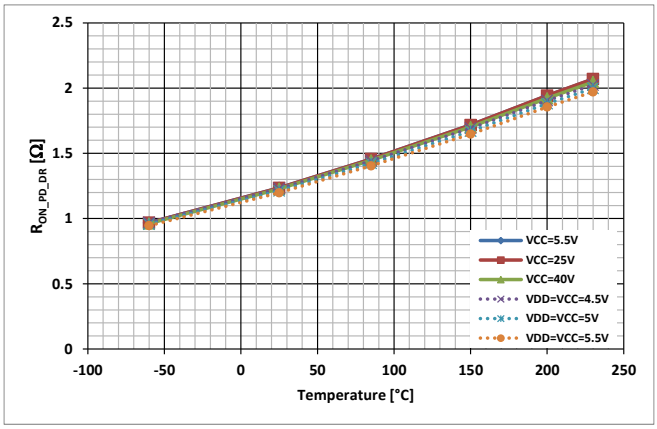


Figure 7. R_{ON} of pull-down driver (PD_DR) versus case temperature (I_{DS}=200mA).

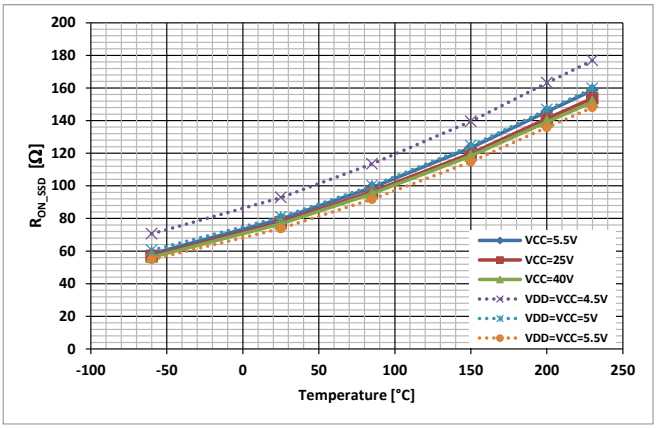


Figure 8. R_{ON} of soft shut down driver (SSD)[12] versus case temperature (V_{DS}=2V).

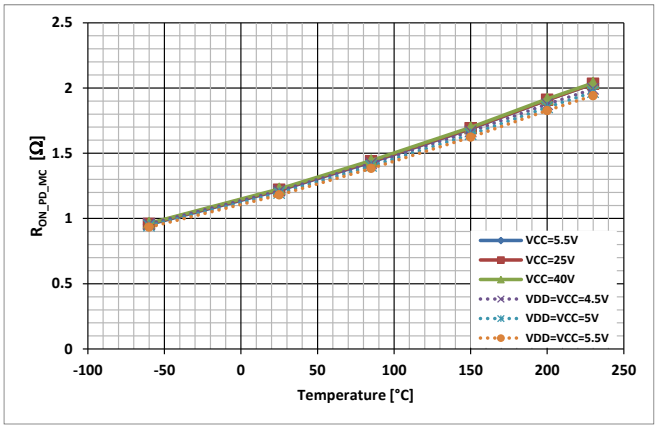


Figure 9. R_{ON} of miller-clamp driver (PD_MC) versus case temperature (I_{DS}=200mA).

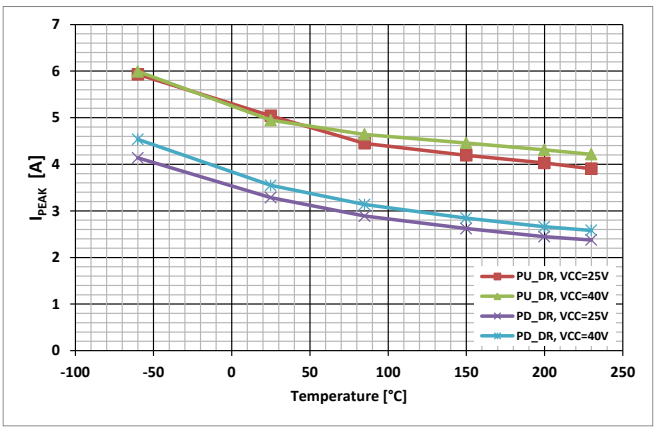


Figure 10. Peak output current of pull-up driver PU_DR and pull-down driver PD_DR versus case temperature (C_{LOAD}=100nF).

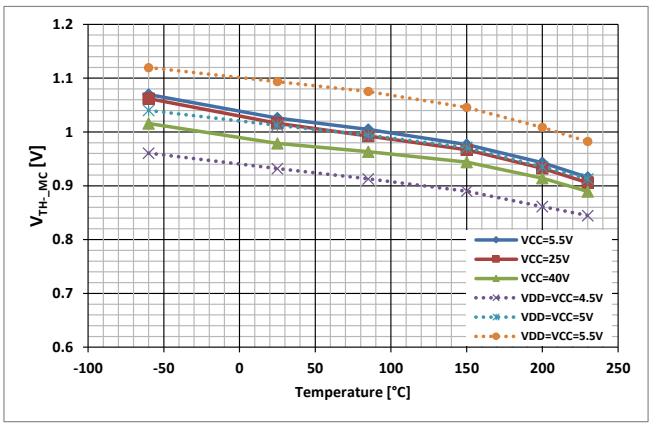


Figure 11. Miller clamp activation threshold voltage versus case temperature.

[12] *R_{ON} SSD calculated with measured current when PD_MC pin is set at 2V while OCP fault is ON*

TYPICAL PERFORMANCE (CONTINUED)

Unless otherwise stated, temperature parameter is "Case temperature" T_C
Graphical legend "VDD=VCC" means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

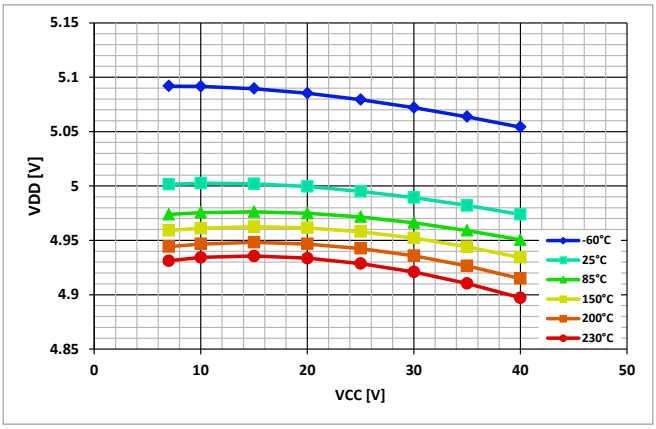


Figure 12. LDO output voltage versus VCC power supply for I_{LOAD}[13]=60mA (in ready mode with IN_PWM=0) VCC in range 7V≤VCC≤40V.

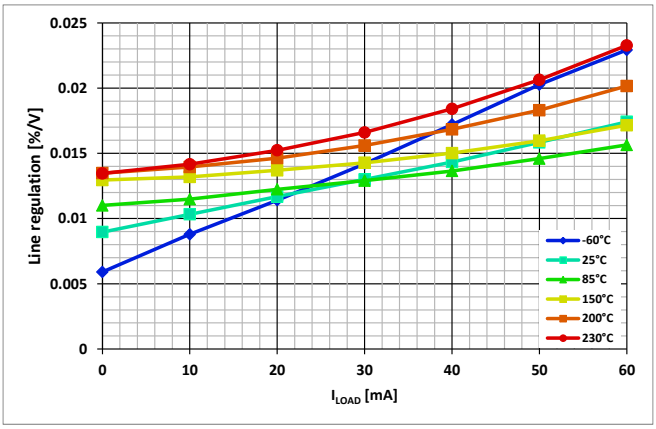


Figure 13. LDO line regulation versus VDD pin external load current for VCC in range 7V≤VCC≤40V (in ready mode with IN_PWM=0).

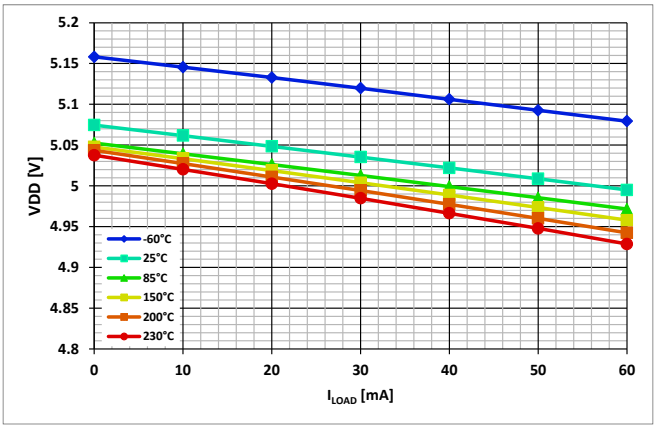


Figure 14. LDO output voltage versus VDD pin external load current for VCC=25V (in ready mode with IN_PWM=0).

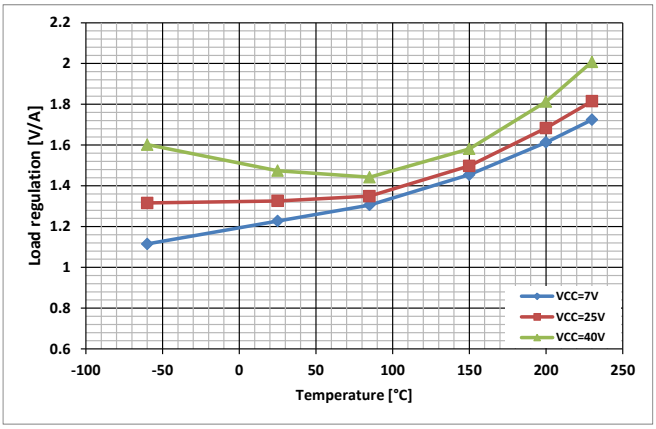


Figure 15. LDO load regulation for I_{LOAD}[13]=60mA versus VDD pin external load current (in ready mode with IN_PWM=0).

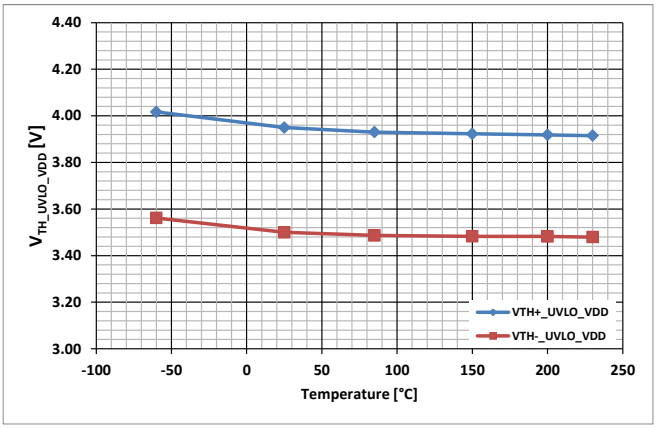


Figure 16. UVLO threshold voltage on VDD versus case temperature.

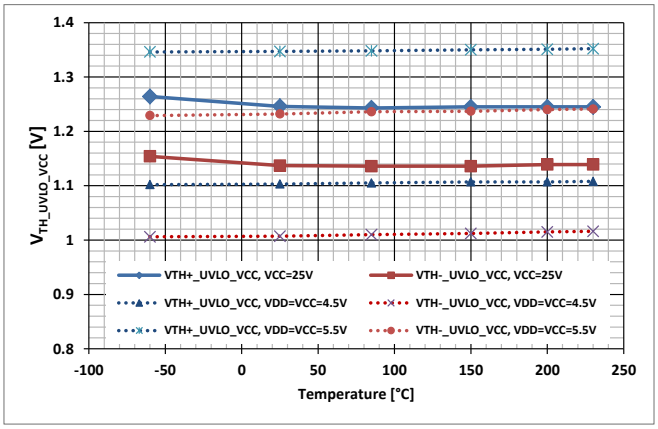


Figure 17. UVLO Threshold voltage on pin UVLO (UVLO VCC) versus case temperature.

[13] *I_{LOAD} is the current sourced by the LDO to the external measurement tool. Note that the LDO is simultaneously sourcing current to internal logic (This internal current can be considered closed to I_{q0} when in ready mode with IN_PWM=0)*

TYPICAL PERFORMANCE (CONTINUED)

Unless otherwise stated, temperature parameter is "Case temperature" T_C
Graphical legend "VDD=VCC" means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

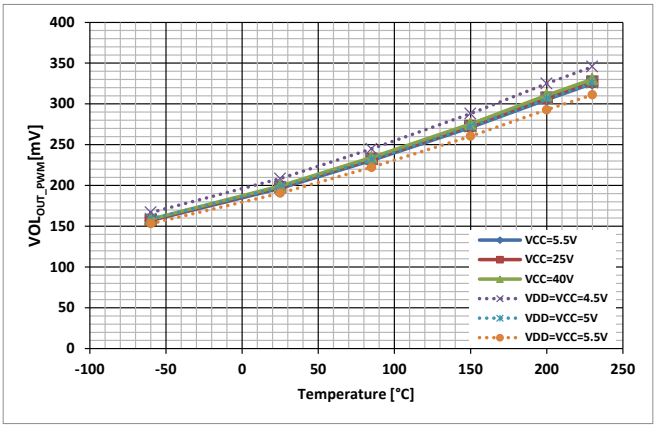


Figure 18. OUT_PWM VOL voltage versus case temperature when DUT is sinking 8mA.

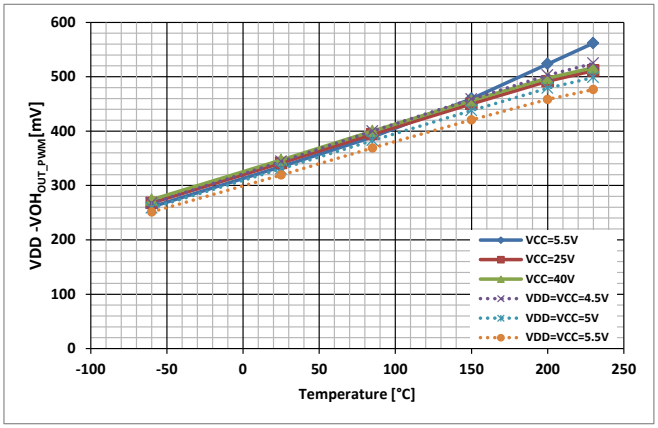


Figure 19. OUT_PWM "VDD-VOH" voltage versus case temperature when DUT is sourcing 8mA.

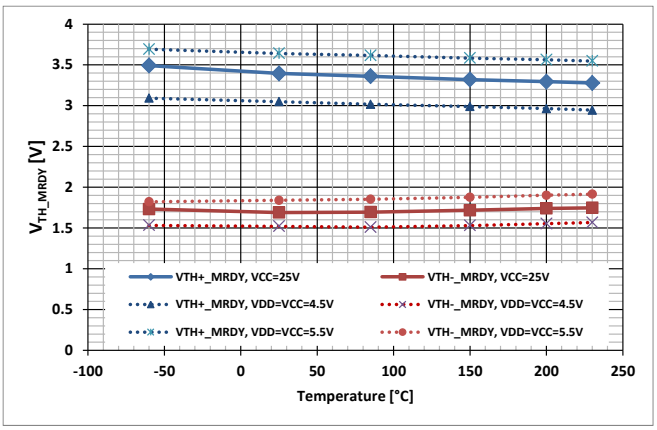


Figure 20. MRDY threshold voltage versus case temperature.

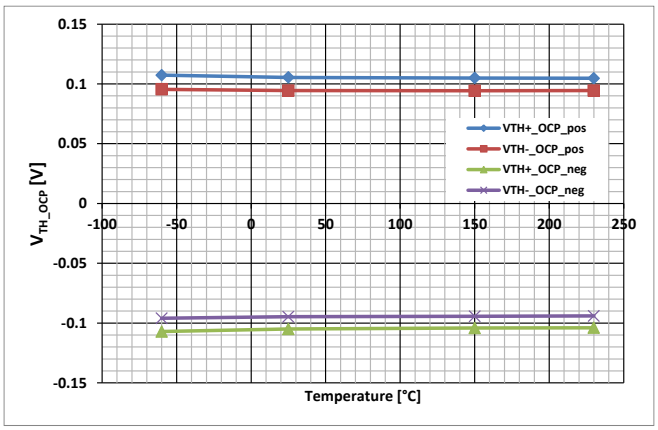


Figure 21. Over current protection threshold voltages versus case temperature at VCC=25V and SNS_S_N at VSS. (Average on 10 devices).

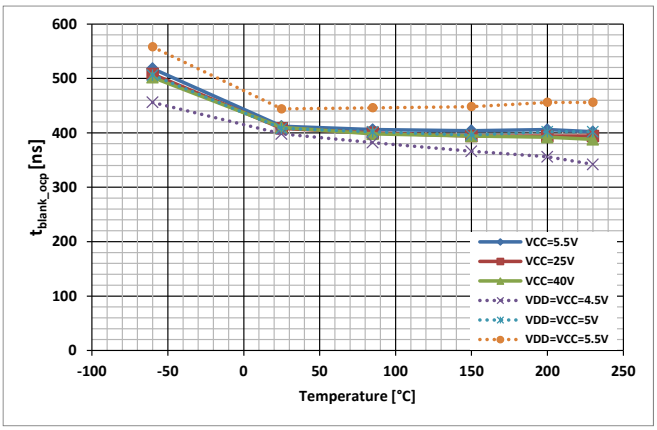


Figure 22. Over current protection blanking time versus case temperature.

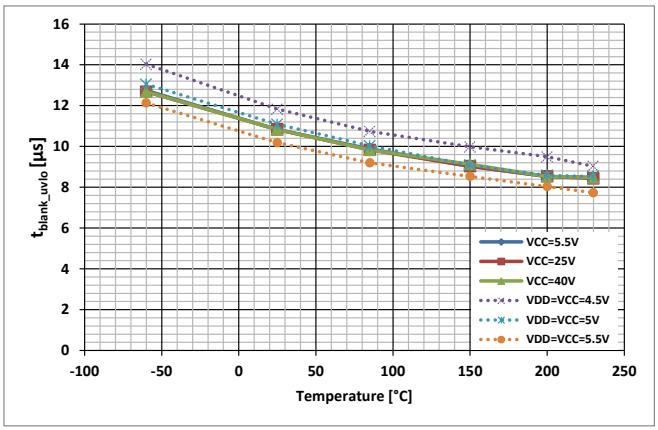


Figure 23. Fault on UVLO pin blanking time versus case temperature.

TYPICAL PERFORMANCE (CONTINUED)

Unless otherwise stated, temperature parameter is "Case temperature" T_C
Graphical legend "VDD=VCC" means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

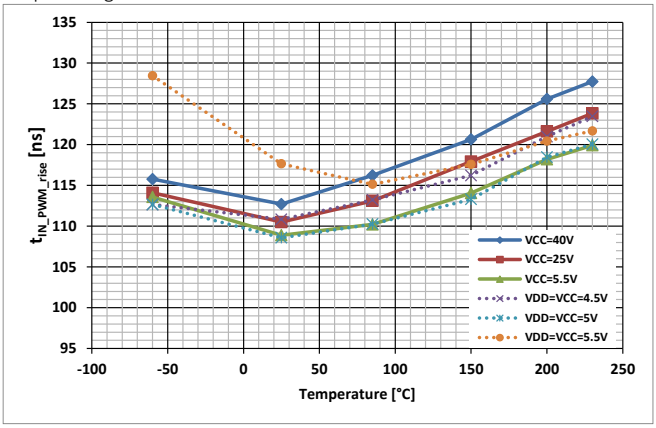


Figure 24. Propagation delay from IN_PWM_P rising (50%) to OUT_PWM rising (10%) versus case temperature (with IN_PWM_N at VSS[14]).

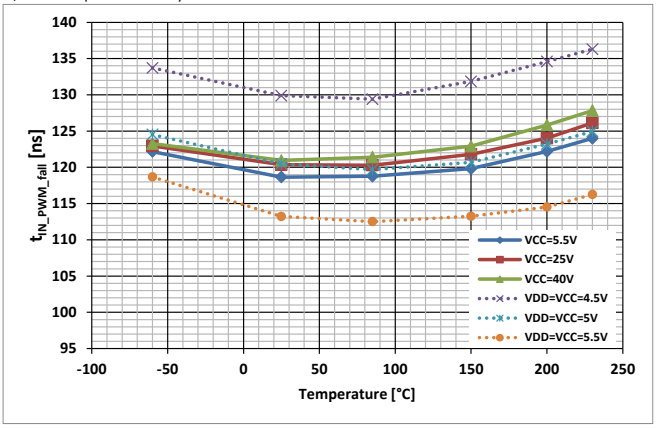


Figure 25. Propagation delay from IN_PWM_P falling (50%) to OUT_PWM falling (90%) versus case temperature (with IN_PWM_N at VSS[14]).

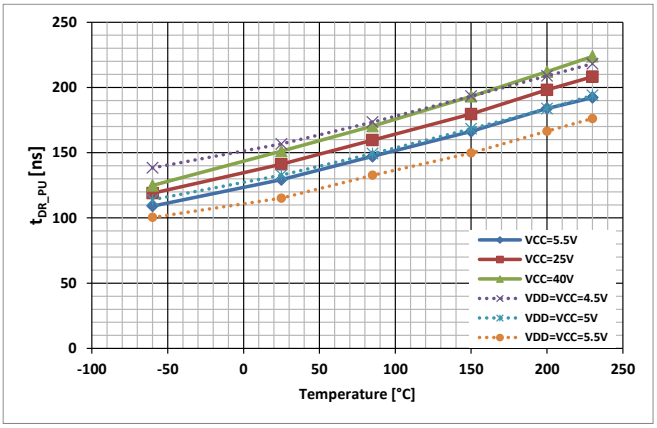


Figure 26. Propagation delay from OUT_PWM rising (67%) to PU_DR rising (10%) versus case temperature.

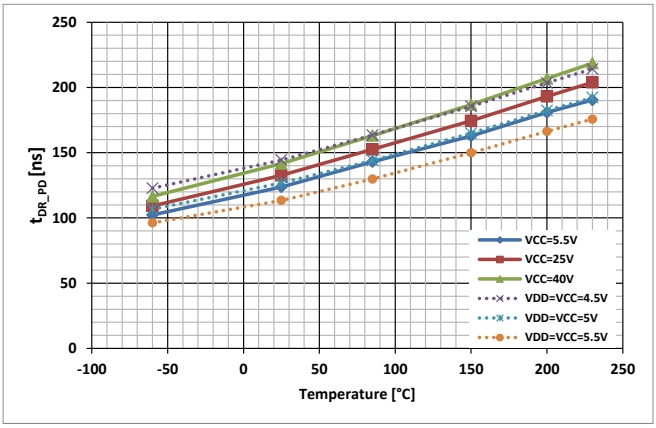


Figure 27. Propagation delay from OUT_PWM falling (33%) to PD_DR falling (90%) versus case temperature.

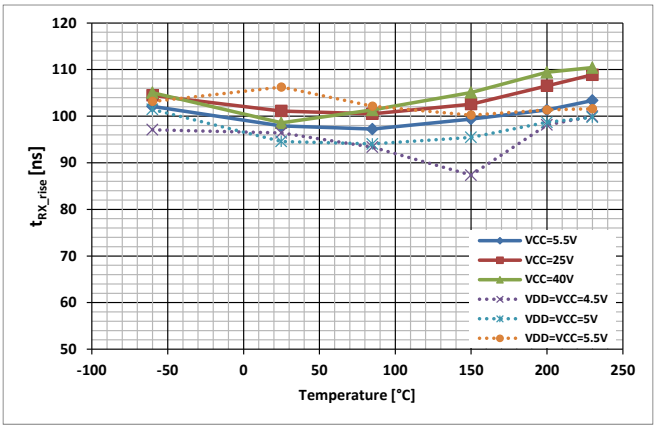


Figure 28. Propagation delay from RX_P rising (50%) to OUT_PWM rising (10%) versus case temperature (with RX_N at VSS[15]).

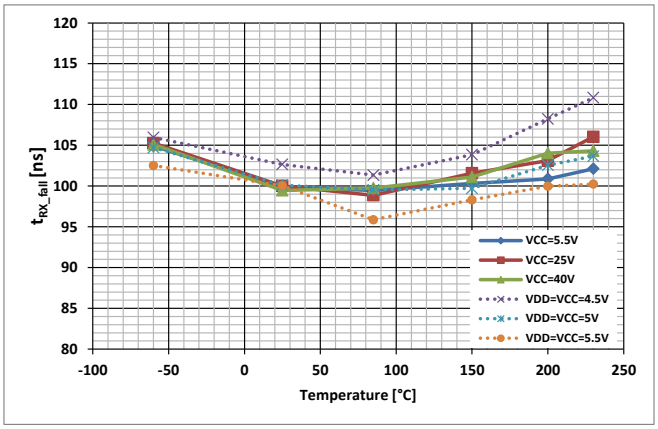


Figure 29. Propagation delay from RX_P falling (50%) to OUT_PWM falling (90%) versus case temperature (with RX_N at VSS[15]).

[14] *In typical application, IN_PWM_P/N is an OOK modulated signal driven by XTR40010 through a pulse transformer. For this measurement a square waveform generator has been used directly connected to IN_PWM_P, with IN_PWM_N at VSS.*
[15] *In typical application, RX_P/N is an OOK modulated signal driven by another XTR26020 through a pulse transformer. For this measurement a square waveform generator has been used directly connected to RX_P, with RX_N at VSS.*

TYPICAL PERFORMANCE (CONTINUED)

Unless otherwise stated, temperature parameter is “Case temperature” T_C
Graphical legend “VDD=VCC” means that VCC is shorted to VDD. If not indicated, VDD is powered by internal LDO.

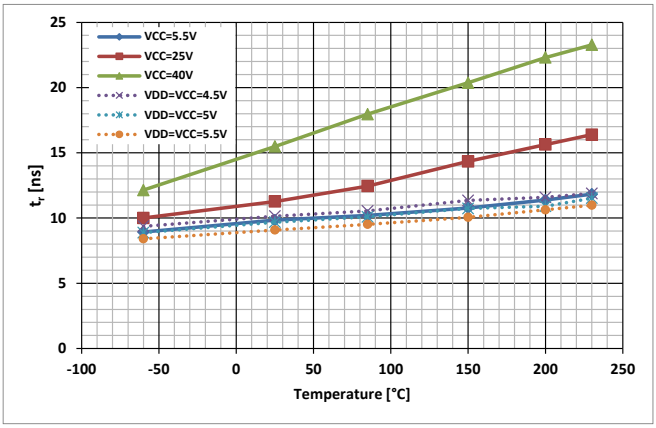


Figure 30. Rise time of PU_DR (delay 10% / 90%) versus case temperature with C_{LOAD}=1nF.

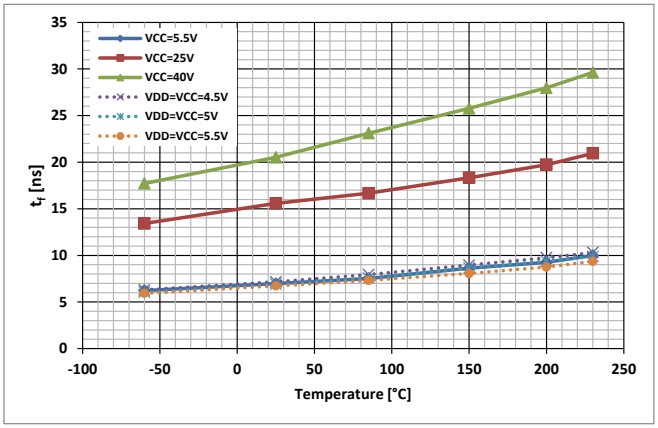


Figure 31. Fall time of PD_DR (delay 90% / 10%) versus case temperature with C_{LOAD}=1nF.

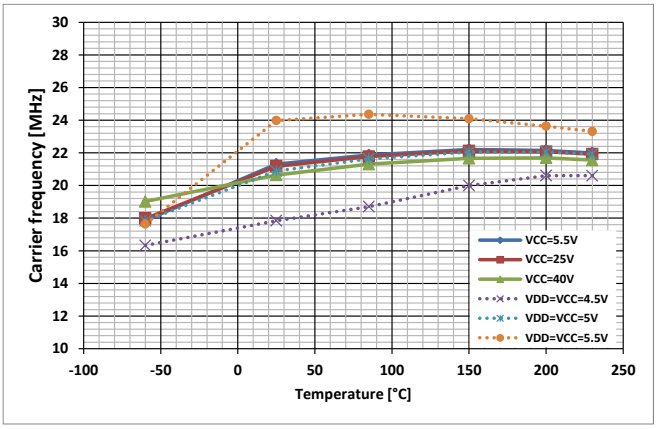


Figure 32. Transceiver OOK carrier modulation frequency versus case temperature.

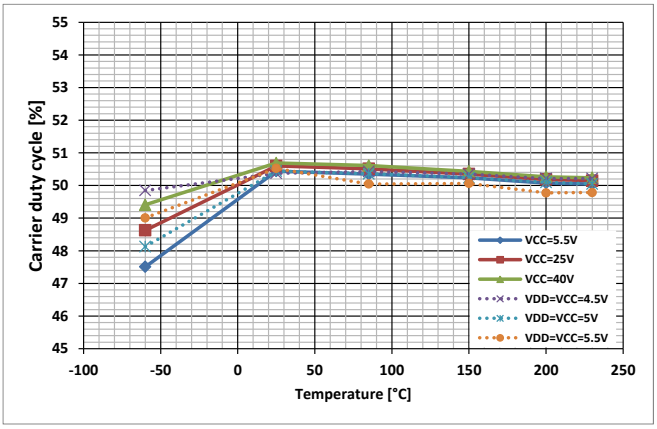


Figure 33. Transceiver OOK carrier modulation duty cycle versus case temperature.

THEORY OF OPERATION

Introduction

XTR26020 is a high-temperature, high reliability intelligent power transistor driver integrated circuit designed to drive normally-Off as well as normally-On Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon power transistors, such as MOSFETs, JFETs, SJTs, BJTs, MESFETs and HEMTs. The XTR26020's main features are:

- Internal 5V linear regulator.
- Cross-conduction protection between high-side and low-side power drivers.
- 4-channel transceiver (2 TX and 2 RX) for isolated data transmission with the microcontroller and between high side and low side drivers
- Pull-up gate-drive-channel (PU_DR) capable of sourcing a peak current of 4A and a 1A continuous current.
- Pull-down gate-drive-channel (PD_DR) capable of sinking 2.4A peak current.
- On-chip Active Miller clamp (AMC) on PD_MC channel with 2.4A current capability.
- On-chip soft-shut-down (SSD) capability that slowly shuts down the power transistor in case of fault.
- Rail-to-rail, positive and negative over-current detection on the source terminals of the power transistor.
- Safe start-up through UVLO (Under Voltage Lockout) function.

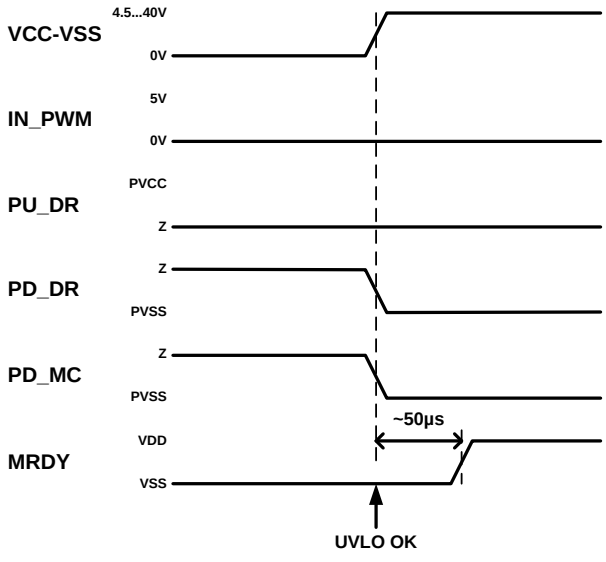
Operation Phases

Startup phase

The startup phase is initialized by the turn on of the power supplies of the circuit VCC and VSS. After having enough voltage on the LDO output (around 3V for the logic to be operational), the PD_DR and PD_MC outputs are pulled-down to PVSS. This is mandatory to guarantee the charge of the bootstrap capacitor during the startup phase. The following checks are done during the startup phase:

- The UVLO on VCC checks if the power supply value is higher than the externally fixed threshold.
- An internal UVLO on VDD checks if VDD is higher than approximately 4V.
- The output gate is checked if it is close to VSS (below 1V versus VSS).

If all those checks are okay, an internal counter with a delay of 50µs is started. This delay secures the correct turn-on of the internal voltage reference. During the startup phase the PD_DR and PD_MC drivers outputs are activated for safe normally on start-up, and the input PWM is blanked (If a PWM signal is received, it is not transferred to the driver outputs). At the end of the counter, the signal MRDY goes to "1". The circuit enters into the functional phase: if a PWM signal is received, it is transferred to the driver outputs.



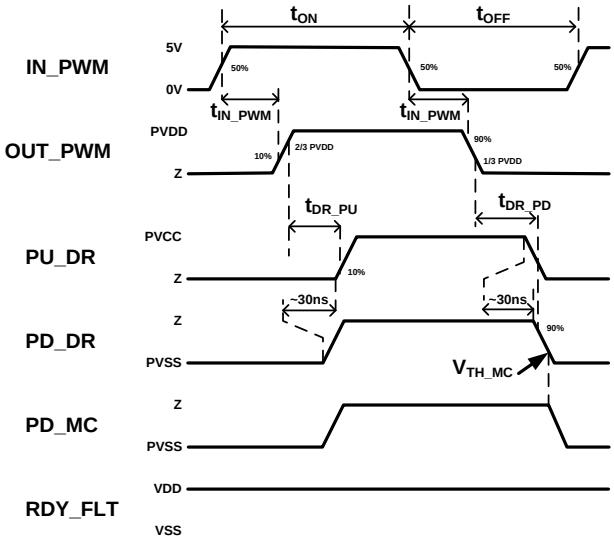
Functional phase

The functional phase starts when the MRDY output flags a "1". In this phase, the circuit is ready to receive the PWM signal from the user (PWM controller, microcontroller…).

When the PWM signal turns on, it is transferred after the propagation delay t_{IN_PWM} from the PWM differential inputs IN_PWM_P and IN_PWM_N to the output OUT_PWM. Then PU_DR driver output is activated when OUT_PWM rising edge reaches 2/3 of VDD and after the propagation delay t_{DR_PU}.
A minimum non-overlapping (of about 30ns) is guaranteed between PU and PD/MC drivers (PU is master).

When the PWM signal turns-off, OUT_PWM signal turns off after propagation delay t_{IN_PWM}. Once OUT_PWM falling edge reaches 1/3 of VDD level, the PU_DR is turned off after the propagation delay t_{DR_PD} and the PD_DR driver is turned-on after the non-overlapping delay. Then, the PD_MC driver is turned-on after checking the output gate to be close to VSS ($V_{GATE}<V_{TH\_MC}\approx1V$).

Note that during this normal operation mode, the soft shut down pull down transistor is always OFF.



Fault phase

The fault phase is initialized if at least one of the following signals flags an error:

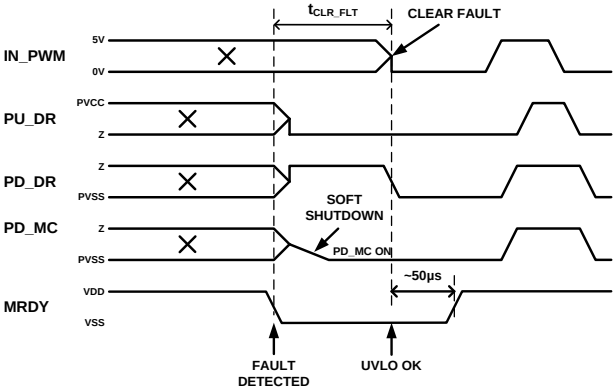
- UVLO on VCC supply versus VSS.
- UVLO on VDD versus VSS
- Over-current detection on the source of the power transistor that persists for a time longer than an internal blanking time t_{BLANK_OCP} (typ 400ns).

Immediately after fault detection MRDY is internally pulled to "0" and this information is sent to the microcontroller through the TX_RDY_FLT transmitter. Then, regardless the states of the inputs, the PU_DR and PD_DR drivers are turned-off and the Soft Shut-Down driver is turned-on. This slowly turns-off the power transistor to avoid high dV/dt and high turn-off current. After checking the output gate to be close to VSS ($V_{GATE}<V_{TH\_MC}\approx1V$), the PD_MC driver is turned-on to strongly maintain the off state.
To get out from this state, two alternatives are possible:

- If the CLR_FLT pin is shorted to VSS, a power supply reset is necessary to clear the FAULT and initialize a new startup phase.
- If a capacitor C_{CLR} is connected between CLR_FLT pin and VSS, a new startup phase starts after a time-out of t_{CLR_FLT} given by:

$$t_{CLR\_FLT}=30k\Omega*C_{CLR}$$

If no capacitor is connected the clear fault time out will be given by the parasitic capacitance on pin CLR_FLT (few pF) times 30kΩ.

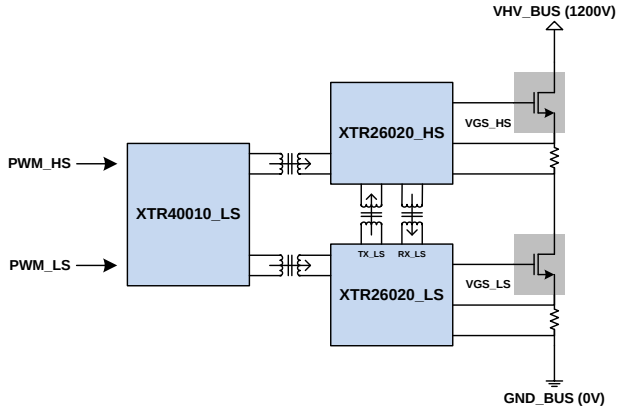


Note that at the first startup of the circuit, when VCC is turning ON, the UVLOs faults are automatically cleared once all supplies are above the defined thresholds. No clear fault event is required in order to operate normally the circuit. However, during operation, if an UVLO event occurs, a clear fault event is required in order to reset the circuit.

Functional Features

Cross conduction protection

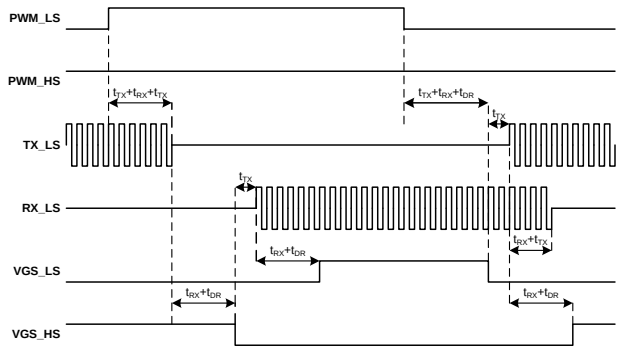
The cross-conduction protection has been implemented to prevent short-circuiting the high voltage power supply through the High Side (HS) and Low Side (LS) power transistors of a half bridge (see figure below).



This is achieved through a bidirectional isolated data communication between the XTR26020 set as a HS driver and the XTR26020 set as a LS driver of the half bridge. The XTR26020 LS is the master and the XTR26020 HS is the slave.

The operation of the cross-conduction protection is shown in the following timing diagrams for two states of the PWM_HS input:

- PWM_HS set to a permanent "1":



When the PWM_LS signal turns-on, after $2*t_{TX}+t_{RX}$ (t_{TX}≈20ns+50ns of Jitter and t_{RX}≈60ns) delay the TX_LS sends a "0" to the RX_HS forcing it to turn-off its PU_DR and to turns-on the PD_DR and then the PD_MC. This takes $t_{RX}+t_{DR}$ delay (t_{DR} is composed of the propagation delay through the driver buffer, the rise or fall time). After checking that the gate of the HS power transistor is nearly discharged (V_{GATE}<1V) using the PD_MC pin, the TX_HS sends a "1" to RX_LS telling that the HS is off and that the LS can safely turn-on after a delay of t_{TX}. Then, the PU_DR LS is turned-on after $t_{RX}+t_{DR}$ delay. Hence, the total turn-off/turn-on delays of the HS/LS are given by:

$$t_{OFF\_HS}=2*(t_{TX}+t_{RX})+t_{DR}$$
$$t_{ON\_LS}=3*(t_{TX}+t_{RX})+2*t_{DR}$$

These delays include a non-overlapping delay of $t_{TX}+t_{RX}+t_{DR}$.

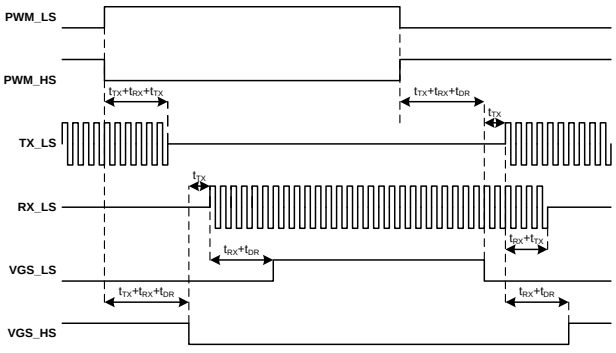
When the PWM_LS signal turns-off, the LS turns-off its PU_DR and turns-on its PD_DR and then its PD_MC after a delay of $t_{TX}+t_{RX}+t_{DR}$. After checking that the gate of the LS power transistor is nearly discharged (V_{GATE}<1V) using the PD_MC pin, the TX_XCOND_LS sends a "1" to the RX_XCOND_HS telling that the HS can turn-on after t_{TX} delay. Finally, the high side turns-on its PU_DR after $t_{RX}+t_{DR}$ delay and receives on its RX_XCOND_LS a "0" after $t_{RX}+t_{TX}$ delay. Hence, the total turn-off/turn-on delays of the LS/HS are given by:

$$t_{OFF\_LS}=t_{TX}+t_{RX}+t_{DR}$$
$$t_{ON\_HS}=2*(t_{TX}+t_{RX})+2*t_{DR}$$

These delays include a non-overlapping delay of $t_{TX}+t_{RX}+t_{DR}$.

In this case, where IN_PU_HS is set to a permanent "1", the pulse transformer that transfers the PWM signal to the XTR26020 HS is not necessary.

- PWM_HS set to $\overline{\text{PWM\_LS}}$ (this could be achieved easily by shorting PWM_HS to PWM_LS and setting POL_TX of the XTR40010_HS to "1"):

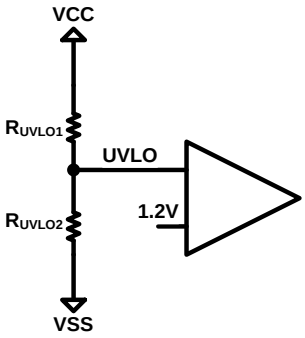


Using complementary signal on PWM_LS and PWM_HS, the same operation is obtained as with a permanent "1" on PWM_HS except that the propagation delay for turn-on from PWM_LS to VGS_LS can be reduced by $t_{TX}+t_{RX}$. This allows to have the same turn-on delay for HS and LS ($t_{ON\_HS}=t_{ON\_LS}$).

The cross-conduction protection can be disabled if the user wishes to manage it externally. To do this both the HS and LS drivers must be set as slave (HS_LSB pin connected to VDD) and the RX must receive a "1" (i.e. RX_P connected to VDD and RX_N connected to VSS).

Under Voltage Lockout (UVLO) operation

The UVLO block checks the value of the external power supply (VCC-VSS), and the internally generated VDD supply versus VSS. A fraction of VDD value is compared to an internal reference of 1.2V versus VSS and an UVLO_VDD flag is set to "1" when the VDD reaches about 3.9V. For the external power supplies, the UVLO block compares an externally fixed threshold through a resistor divider to an internal reference of 1.2V versus VSS:



To simplify the equation for the computation of the UVLO threshold voltage V_{TH_UVLO}, we consider VSS=0V. The V_{TH_UVLO} is obtained in terms of R_{UVLO1} and R_{UVLO2} as follows:

$$V_{TH\_UVLO}=\frac{R_{UVLO1}+R_{UVLO2}}{R_{UVLO2}}\cdot 1.2V$$

The current that can be tolerated (100µA for example, it must be high enough compared to leakage current) in the resistor divider can give the value of R_{UVLO2} using:

$$R_{UVLO2}=\frac{1.2V}{100\mu A}=12k\Omega$$

Then, for V_{TH_UVLO}=15V, the R_{UVLO1} is obtained:

$$R_{UVLO1}=\left(\frac{V_{TH\_UVLO}}{1.2}-1\right)\cdot R_{UVLO2}=138k\Omega$$

The UVLO pin is internally clamped to VDD+0.7V with a maximum current sink of 1mA.
The UVLO thresholds on VDD and VCC have an internal hysteresis of about 10% when the power supply goes down after being up and higher than the UVLO thresholds defined above.
If this feature is not used, the UVLO pin must be pulled-up to VDD.

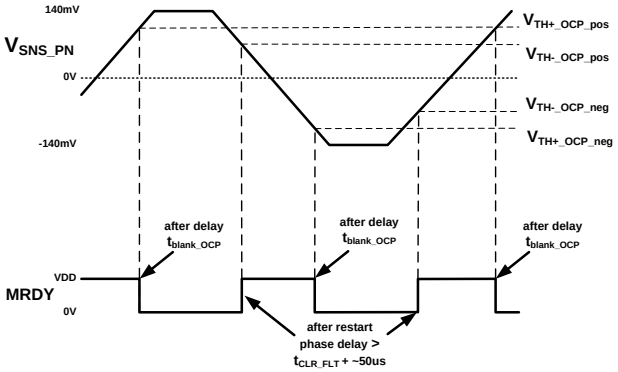
Over-current detection

The source or gate current is permanently measured using the differential voltage V_{SNS_PN} between SNS_S_P and SNS_S_N created by the sense resistor R_{SNS} and compared to an internal voltage reference of about 100mV. In the case of damage on the poser transistor or due to short-circuit in a half-bridge, the current should be higher than the fixed threshold indicating source failure for the circuit. The source or gate over-current threshold I_{TH} is given by:

$$I_{TH}=\frac{100mV}{R_{SNS}}$$

The current sense is functional at any common-mode voltage between VCC and VSS (rail-to-rail) and for both positive and negative current flowing to or from the source of the power transistor. In order to avoid false over-current detections due to spikes during the switching of the driver outputs, an internal blanking time t_{blank_OCP} = 400ns is implemented.

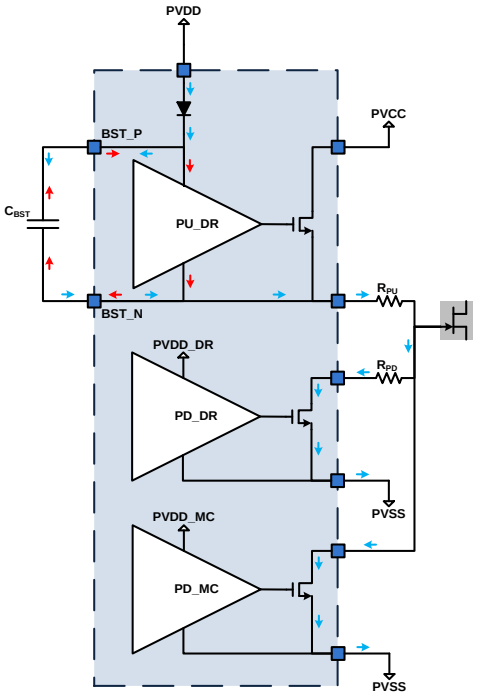
The current sense comparator can also be used for any other protection purpose such as gate/base current sense for fatigue detection or to implement a thermal shut-down with external temperature sensor.

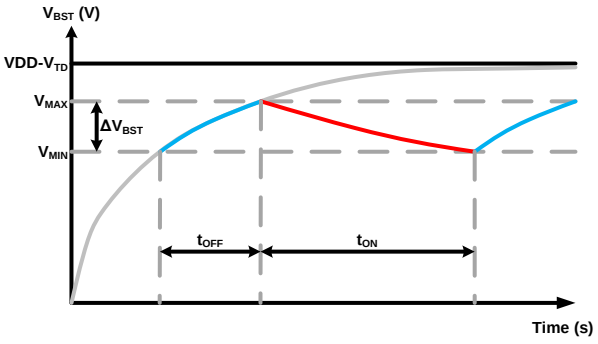


Bootstrap capacitors

The bootstrap capacitor value can be selected taking into account three conditions:

- The bootstrap capacitor C_{BST} is discharged in the PU_DRx driver during the ON time t_{ON} as shown by the red arrows in the figure below.





As shown in the graph above, in steady state, the voltage-drop ΔV_{BST} on C_{BST} during discharge (red curve, ON time t_{ON}) is given by:

$$\Delta V_{BST} = (Iq*t_{ON}+C_{eq}*V_{MAX})/C_{BST}$$

where Iq=250µA is the quiescent current delivered from BST_P to the pull-up driver, C_{eq}≈500pF is the equivalent capacitor that must be charged by BST _P up to the voltage V_{MAX}, t_{ON}=1/fr-t_{OFF}, and fr is the PWM frequency.

To have a first guess for C_{BST}, we consider the extreme values for V_{MAX} = VDD-V_{TD} (V_{TD} is the threshold voltage of the bootstrap diode), and ΔV_{BST}=300mV to ensure V_{MIN} > 4V, which is the threshold to turn-on the integrated charge pump. Indeed, the integrated charge pump has been designed to be able to maintain the on state permanently (PWM DTC 100%). It is not able to provide enough charge to the bootstrap capacitor when the PWM signal is switching. Therefore, the following condition on C_{BST} is obtained, which gives a lower limit:

$$C_{BST} > [Iq*t_{ON}+C_{eq}*(VDD-V_{TD})] / \Delta V_{BST} \qquad (1)$$

For VDD-V_{TD}=4.3V, fr=50kHz, and t_{ON}=19µs (t_{OFF}=1µs), C_{BST} must be higher than 23nF. As this is an extreme value, we recommend taking at least two times this value to reduce the voltage ripple ΔV_{BST}.

- The bootstrap capacitor C_{BST} is charged for the first time during the startup time given by the rise time of the power supply and the 50µs delay fixed by the startup counter. The charging path is, as described in the figure above with the blue arrows, going from the 5V versus VSS power supply PVDD via the integrated bootstrap diode, then the external R_{PU}, and finally the PD_MC driver in parallel with the R_{PD} and the PD_DR driver. Hence, C_{BST} must fulfill the following condition to guarantee its total charge during the startup, which gives an upper limit:

$$C_{BST} < 50\mu s/(3*R_{PU}) \qquad (2)$$

As the on resistances of the PU, PD, MC transistors are less than 2.7Ω, they are neglected compared to R_{PU} and R_{PD}. For R_{PU}=20Ω, C_{BST} must be smaller than 833nF.

In steady state, as shown in the graph above, the voltage drop ΔV_{BST} on C_{BST} during the charge (blue curve, OFF time t_{OFF}) is given by:

$$\Delta V_{BST}=(VDD-V_{TD}-V_{MIN})*(1-\exp[-t_{OFF}/(R_{eq}*C_{BST})])$$

where R_{eq} is given by:

$$R_{eq}=(R_{PU}+R_{PD})*t_{MC}/t_{OFF}+R_{PU}*(t_{OFF}-t_{MC})/t_{OFF}$$

From the equation of ΔV_{BST} during the charge, the following condition on R_{eq} is obtained:

$$R_{eq} < -t_{OFF}/(C_{BST}*\ln[1-\Delta V_{BST}/(VDD-V_{TD}-V_{MIN})]) \qquad (3)$$

For V_{MIN}=4V, t_{MC}=100ns, t_{OFF}=1µs, and C_{BST}=47nF, R_{eq} must be smaller than 32Ω. With R_{PU}=R_{PD}=20Ω (R_{eq}=22Ω), fr=50kHz, t_{OFF}=1µs, and C_{BST}=47nF, the following ripple characteristics are obtained:

$$\Delta V_{BST} = 150mV,\ V_{MAX} = 4.21V,\ V_{MIN} = 4.06V$$

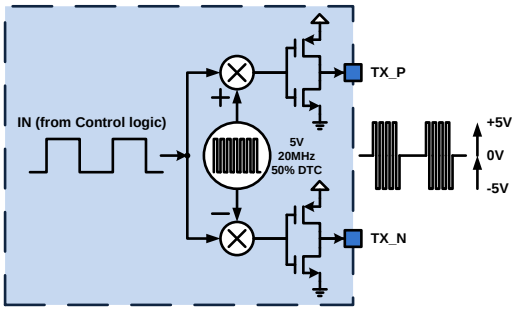
The voltage across the bootstrap capacitor V_{BST} is protected against over-voltage to prevent exceeding 6V, which could damage the part. While the V_{BST} voltage is monitored permanently, as soon as it exceeds 6V threshold, a discharge path from the bootstrap capacitor top plate BST_P to VSS is activated through an internal resistor of about 10kΩ. This protection is blanked for 2µs after each PWM rising/falling edge to avoid bad activation of this protection due to switching noise. Hence, for PWM frequency below 100kHz, no additional external protection is needed. If the PWM frequency is around or higher than 100kHz, it is recommended to add a 6V clamping diode to avoid damaging the part.

Transceiver

The XTR26020 implements a 4-channel isolated data transceiver with 2 transmitters (TX_XCOND and TX_RDY_FLT) and 2 receivers (RX_XCOND, RX_PWM). The galvanic isolation is achieved by an external magnetic transformer for each channel signal.
In the following sections, only one transmitter and one receiver will be described.

TX operation

The transmitter is composed of the following functions (as shown in the figure below):



- Oscillator: This block generates a clock with typical oscillation frequency of 20MHz.

- Modulator: This block implements a classical On-Off Keying (OOK) modulation using the clock generated by the oscillator and the digital input signal coming from the control logic block. If a digital "1" is sent to the input of the transmitter, it will be transferred as a differential ±5V at the output pins **TX_P/TX_N** (i.e. one of the output at VDD while the other one is at VSS, then, it changes to VSS and VDD respectively). On the other hand, a digital "0" is transferred as a differential 0V at the output pins **TX_P/TX_N** of the transmitter (both outputs are in fact at VSS).

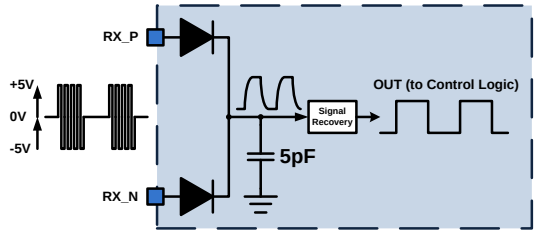
- The output buffer: It consists of several inverters with a typical R_{ON} of 15Ω for the last stage (NMOS or PMOS). This buffer is driven by two complementary signals generated by the modulator. These signals have a duty cycle very close to 50% to limit the DC current in the primary inductance of the pulse transformer. This DC current could induce a magnetic field that would saturate the magnetic core and compromise the data transfer.

Transmitter truth table

IN (from Control Logic)	TX_P	TX_N
0	0	0
1	CK	/CK

RX operation

The receiver implements a classical full-wave rectification to demodulate the signal received on the pulse transformer secondary winding (as shown in the figure below). The signal recovery block aims to ensure immunity versus possible high dv/dt, which induces common mode current from one side of the pulse transformer to the other side. This common mode current can induce errors in the data transmission from the transmitter side to the receiver side. When a dv/dt event happens, it is detected by this block. During the dv/dt event the output data is kept at its value just before the dv/dt event. After the dv/dt event, the input data is transferred to the output.



Receiver truth table

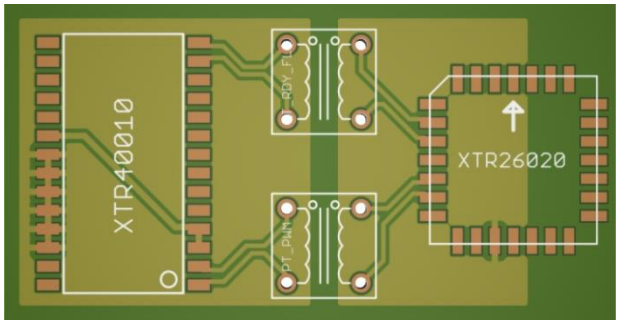
RX_P	RX_N	OUT (to Contol Logic)
0	0	0
0	1	1
1	0	1
1	1	forbidden

Pulse transformer

The pulse transformer specifications and design guidelines are given in the application note “Pulse Transformer Design Guidelines” (AN-00371-13).

TX/RX routing guidelines

As the TX/RX signals are clocked at 20MHz with sharp transitions, a special care must be taken for their routing to and from the pulse transformers. If no care is taken for their routing, a strong coupling between different TX or RX signals may affect dV/dt immunity. Indeed, if the RX input traces have asymmetrical parasitic coupling capacitances to noisy traces in addition to a dV/dt event, a voltage difference can appear between RX inputs leading to a possible false transient state. It is also recommended to keep enough distance between the pulse transformers to avoid magnetic coupling between neighboring magnetic cores. An example of good practice for a PCB routing between XTR26020 and XTR40010 is given hereafter:

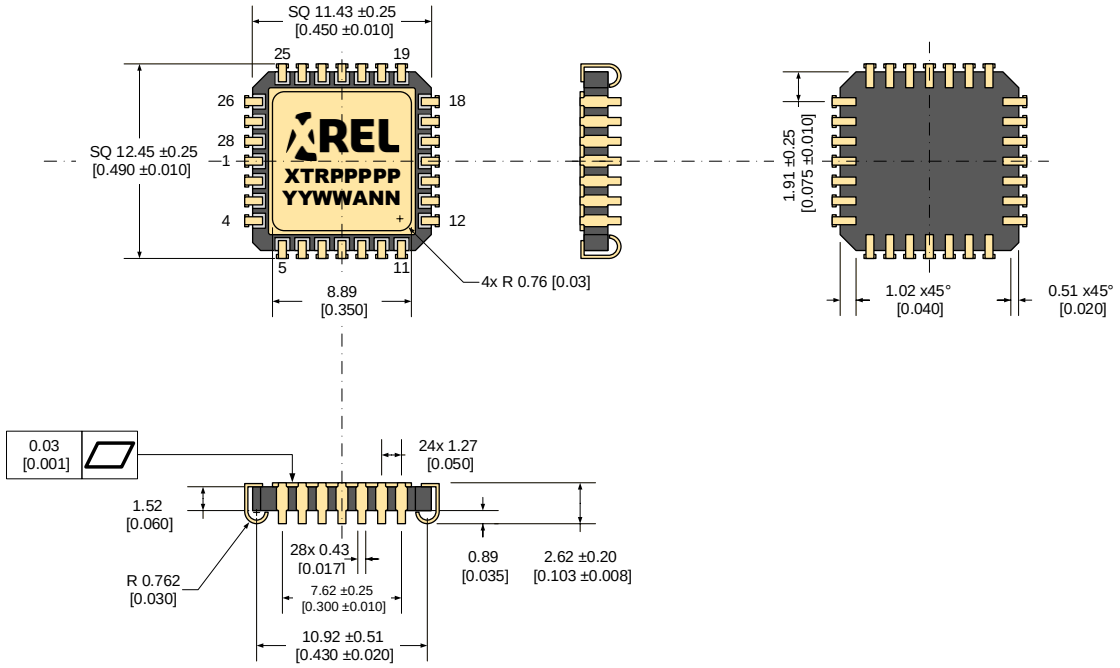


If for any other constraints it is not possible to optimize the routing as indicated above, it is recommended to add pull-down resistors to **VSS** in the range of 1kΩ to 10kΩ on each input of the RX and a capacitor in the range of 5pF to 10pF between differential RX inputs.

PACKAGE OUTLINES

Dimensions shown in mm [inches].

J-Formed Leaded Chip Carrier LJCC28



Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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