CoaXPress2 Multi-Link Multi-Stream Device IP

Videostreaming at up to 100 Gbps

Xilinx & Intel FPGA Core IP

CoaXPress2 Device IP from EASii-IC enables the transmission of video streams from multiple cameras on single or multiple coaxial cables at a maximum transfer rate of 100 Gbps over 15 meters or at a transfer rate of 10 Gbps over 200 meters with 8 cables. Each coaxial cable provides a high-speed downlink connection video transfer rate from 1.25 Gbps to 12.5 Gbps and a low-speed uplink connection from 20.83 to 41.66 Mbps for communication and control.

ABOUT COAXPRESS

CoaXPress standard defines a cost effective and easy interfacing between video devices and acquisition hardware over RG59 and RG6 coaxial cables. It enables hot-plug of devices and 24V power-over-cable with up to 13 Watts per cable.

A device can support multiple cameras of many video stream formats. Video streams are sent to a host at a selectable high-speed downlink connection rate from 1.25 Gbps to 12.5 Gbps per cable, with up to 8 cables per device to increase the total bandwidth to 100 Gbps.

Devices can be controlled from a host through the uplink connection up to 41.66 Mbps. The standard also provides a low latency, accurate trigger interface between device and host.

CoaXPress supports GenICam international standard, providing a generic programming interface for all kinds of cameras regardless of the interface technology.

APPLICATIONS AND DOMAINS

Vision systems requiring

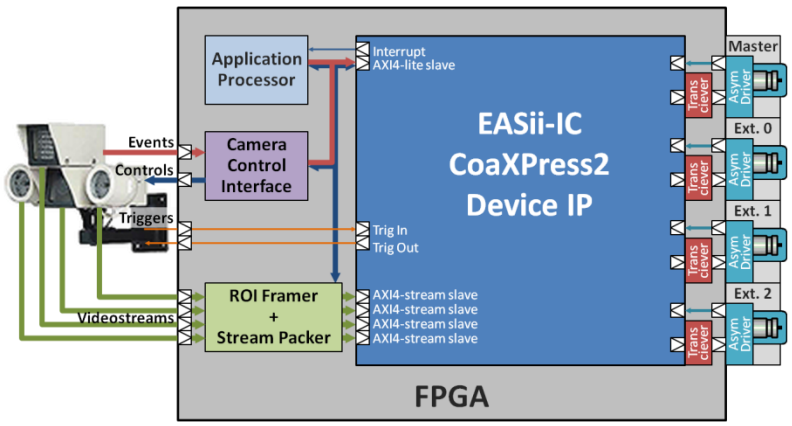
- High-resolution and high-speed digital cameras
- Real-time image acquisition
- Pixels on target
- Long distance cables with excellent EMI/EMC performance

Domains

- Machine vision
- Military and aerospace
- Aerial mapping and traffic management
- Security

TYPICAL USE CASE

EASii-IC Device Core IP can be embedded in a Xilinx 7 FPGA with its application processor, camera control interface and pixel stream packer.



EASII IC CXP DEVICE CORE IP FEATURES

- **JIAA CXP-001-2018 CoaXPress 2.0** compliant
- **Selectable downlink connection rates**, from 1.25 Gbps to 12.5 Gbps, up to 8 coaxial connections per Device IP
- **Supports multiple video-streams**, up to 256 independent stream IDs
- **Supports all GenICam compliant image formats**: rectangular and arbitrary shaped, area and line scan, single and multi tap, multiple regions of interest, all standard pixel formats
- **Trigger in/out level type and pulse type interfaces** with maximum jitter of 8 ns and constant uplink latency of 1.7 µs or 3.4 µs
- **Event messages** from device to host
- **Heartbeat** for time clock transmission from device to host
- **AXI4-lite slave processor interface** for application specific control between host and cameras (optional)
- **Up to 4 AXI4-stream slave interfaces** for video streams, 32/64/128/256-bit data bus
- **Xilinx 7-Series/UltraScale compatible, Intel 10-Series compatible, IP-XACT support**

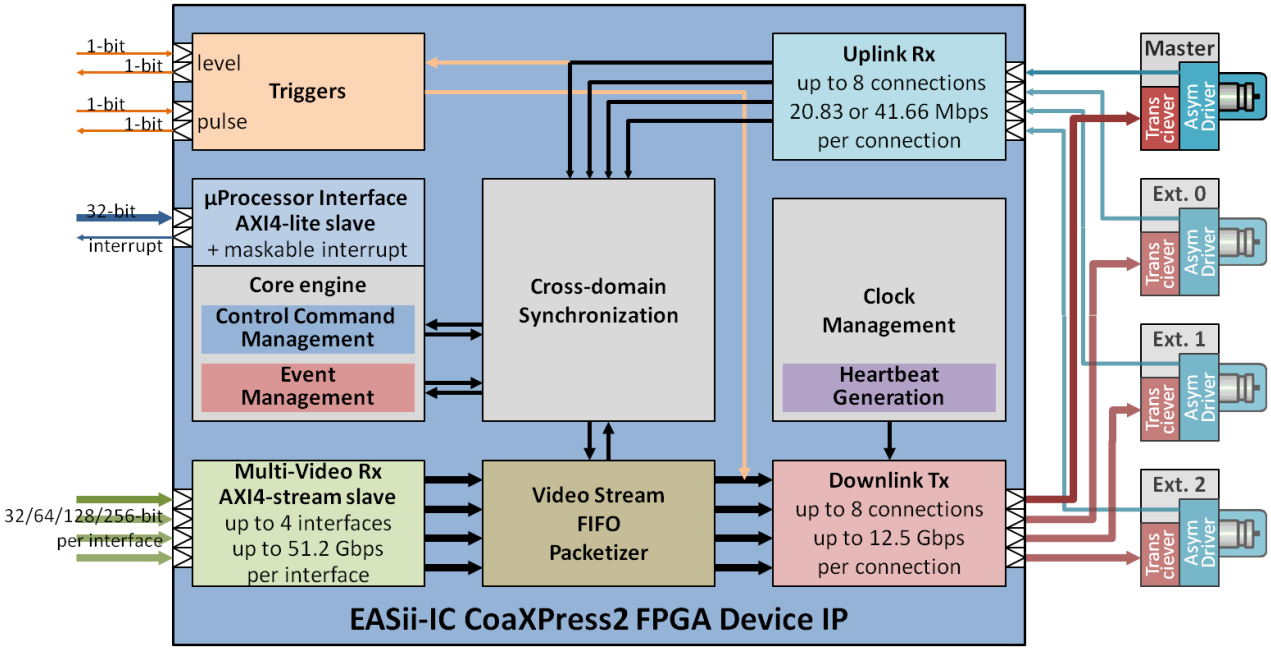
PRODUCT DETAILS

- Master connection with up to 7 extension connections connected to a single host
- Embedded connection management: sync, init, soft-reset
- Dynamic reconfiguration: bit-rate, number of connections
- Embedded CRC management
- Video-stream data packet size up to 4096 bytes
- Up to 4 video-stream interfaces AXI-stream slave, 32/64/128/256-bit per interface, running at up to 200 MHz (independent from system-clock)
- Embedded management of triggers
- Processor interface to send application specific event messages from device to host
- Embedded management of heartbeat
- Embedded bootstrap registers
- µProcessor interface AXI4-lite slave 32-bit

DELIVERABLES

- Single or multi-use license
- Encrypted source code: VHDL RTL with synthesis scripts for Xilinx Vivado or Intel Quartus
- Comprehensive documentation package: specification, integration, IP-XACT component, etc.
- Example designs

CORE IP ARCHITECTURE



CORE IP RESOURCES

Examples on Kintex UltraScale, single AXI4-Stream interface

CoaXPress configuration	CXP6_X1	CXP12_X1	CXP6_X4	CXP12_X4
AXI4-stream data width	32-bit	64-bit	128-bit	256-bit
Flip-Flops	9.5k	9.7k	17.1k	18.5k
LUT	8.3k	8.7k	16.7k	18.8k
BRAM 36Kb	11	13	24	32
DSP48	1	1	1	1

- Transceiver logic and reconfiguration are not included
- Numbers are subject to change depending on the FPGA target, features selection and future evolutions

CONTACT US

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